Optimized wet processes and PECVD for high-efficiency solar cells

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Introduction

The semiconductor industry considers wet cleans to be critical surface preparation steps. The Si/SiO_2 interface, for example, is very critical to achieve high gate oxide integrity and avoid leakage or stacking faults. Similarly, the solar industry has seen the value of wet processes to achieve best cell performance. In this study, we highlight the effect of pre-cleans, texturization and final cleans on cell parameters. We also studied the importance of coupling these wet cleaning and texturization steps with the PECVD steps to achieve the film quality required for highest solar cell efficiency.

Experimental

Wet chemical processes were conducted on a fully-automated GAMA Solar™ etching and cleaning station. Mono-crystalline n-type wafers were used for this study as part of HIT solar cell development efforts. Wafers were pre-cleaned in DIO3™ or SC1 and then texturized in a standard KOH/IPA process. In certain runs, proprietary process was applied to round the pyramid's peaks. The wafers were then processed in an advanced HF/HCl step prior to placement in the PECVD tool. Different PECVD splits were conducted to develop optimum process conditions.

Results and Discussion

Heterojunction (HIT) cells and n-type wafers are getting more traction as a technology to achieve the industry's goal of developing high efficiency, low cost solar cells [1,2]. Sanyo and Sunpower have been using n-type wafers for many years. Recently, all major R&D centers and several companies have published articles about using n-type wafers, which generally have higher lifetimes than p-type silicon, for cell processing. N-type wafers' long diffusion length and high lifetime result in higher cell efficiency, while boron-doped p-type wafers show lifetime degradation due to formation of boron-oxygen defects upon illumination [1-4]. We studied the effect of surface conditioning and the coupling of these surface preparation techniques and PECVD processing to produce high efficiency solar cells.

A. Effect of Pre-cleans Various pre-clean processes were tested to determine their effect on the texturization step. Several wafers were processed in DIO3 and SC1. The results showed that the wafers processed in DIO3 consistently gave a higher Si etch (Figure 1). The wafers also looked more uniform visually, with fewer fingerprints and scratches. SC1 did not show any significant advantage over the as cut wafers. Reflectance at 950 nm wave length for all wafers processed for BKM+50% was <10% (>10% at BKM conditions).

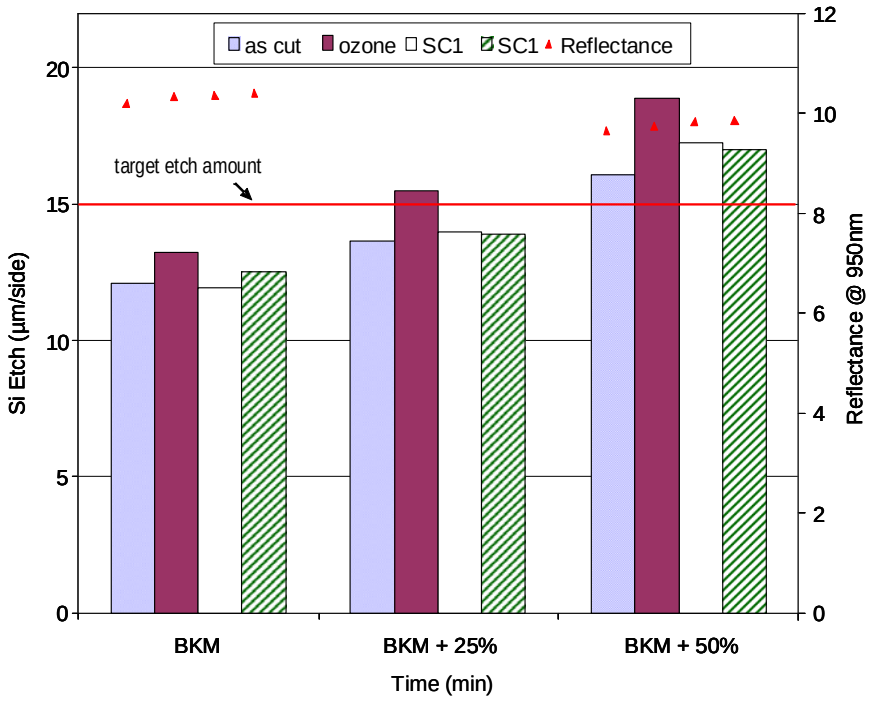

Figure 1: Si etch and reflectance versus various pre-clean processes.

Table 1: Surface metal levels after different final cleans using standard and modified HF/HCl mixtures

Parameter	RL	Sample Identification / Site			
11 Elements on 200mm or smaller Bare Wafers by VPD (2-4 Samples)		**BC**	**BC-C**	**BNC**	**BNC-C**
Units: 1E10 atoms/cm2					
Aluminum (Al)	0.09	37	*	36	*
Calcium (Ca)	0.2	50	2.2	38	2.8
Chromium (Cr)	0.02	1.7	*	14	0.08
Copper (Cu)	0.02	63	*	2300	0.17
Iron (Fe)	0.09	10	0.22	35	0.25
Magnesium (Mg)	0.09	22	1.0	77	1.1
Nickel (Ni)	0.09	0.24	*	1.2	*
Potassium (K)	0.09	6.4	1.3	130	2.5
Sodium (Na)	0.09	17	0.65	8.8	0.74
Titanium (Ti)	0.09	0.84	0.19	3.0	0.24
Zinc (Zn)	0.09	1.5	0.12	3.4	0.53

* = Analysis revealed that the analyte was not found at or above the reporting limit. RL = Reporting Limit

Report Notes: Copper on the surface of wafer BNC is high relative to other three wafers.

B. The effect of Final cleans Special attention has to be made to the final clean prior to PECVD. Typical tools in solar lines leave metal signature on the wafers that is responsible for low minority carrier lifetime. High levels of metals on production wafers in an advanced fab from two different production tools are shown in Table 1 (splits BC and BNC). A specially designed HF/HCl process was applied to the wafers that resulted in significantly lower metals on the wafers' surface as can be seen from Table 1 (splits BC-C and BNC-C). Higher lifetime values (> 1000 µs) were obtained on these wafers after the special HF/HCl step.

C. Effect of PECVD Deposition Conditions These factors were considered when processing the W, S, and C wafers. S wafers were slurry wire-cut while C and W were diamond wire-cut. Wafers were textured in the standard KOH/IPA process and no rounding step was done. The texturization pattern and pyramids shape are shown in Figure 2. Wafers from both W and S types were processed

at the same time. Yet, the pyramid bases were larger for S wafers than those obtain for the W wafers.

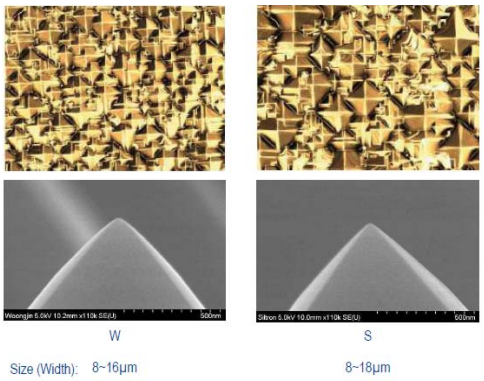

Figure 2: pyramid patterns after standard KOH/IPA texturization for different wafer types (slurry and diamond-cut).

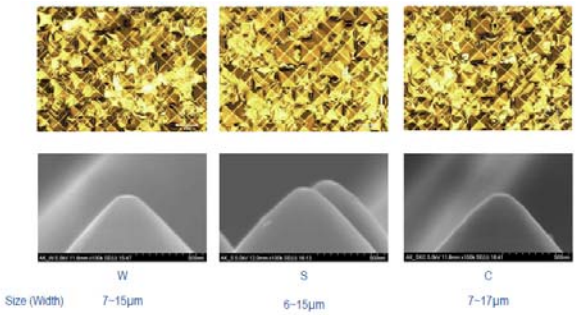

Figure 3: pyramid patterns after standard KOH/IPA texturization for different wafer types (slurry and diamond-cut).

Further optimization of the standard texturization process produced a relatively smaller pyramid base and data is shown in Figure 3. The base of the W wafers ranged from 7-15 μm and the S wafers ranged from 6-15 μm. Another group of wafers was tested as well (wafers C) whose base ranged from 7-17 μm. A secondary process was then conducted on all the wafers to round the sharp peaks of the pyramids for better film deposition and conformity. The results are also shown in Figure 3. For optimum PECVD i-layer deposition, the desired radius of curvature was ~10 μm.

Table 2 shows the results of the different PECVD processes used for optimization. Lifetime and Voc were measured. Voc is the open-circuit voltage - the maximum voltage available from a solar cell which occurs at zero current. As expected, the Voc, is directly related to cell lifetime: the higher the lifetime, the higher the Voc for any wafer and any process. The data also show that different PECVD processes produce different results for lifetime and Voc for the same wet-processed wafers. Therefore, it is important then to tune the PECVD to match a wet process that produces well-texturized and clean wafer in order to maximize the Voc. In addition, the results in Table 2 also show that pyramid rounding further enhances the minority carrier lifetime and Voc.

Table 2: Effect of PECVD deposition conditions on the minority carrier lifetime and implied Voc.

Process	Lifetime (μs)					Implied Voc (mV)				
	Not Round Texture (1st Demo)		Round Texture (2nd Demo)			Not Round Texture (1st Demo)		Round Texture (2nd Demo)		
	W	S	W	S	C	W	S	W	S	C
1	305	335	252	270	311	666	673	660	663	671
2	769	998	893	1002	1004	706	716	711	716	715
3	872	1136	1302	1386	1278	710	720	724	727	724
4	864	694	1424	1605	1651	711	704	726	730	729
5	1026	668	1496	1943	1701	716	702	728	734	731
6	660	–	907	1088	1177	701	–	712	719	722
7	939	–	1105	1169	435	714	–	720	722	684

Another set of experiments was conducted to confirm the importance of coupling the wet process conditions with the PECVD conditions to achieve the highest possible electrical parameters, such as efficiency. Wafers were processed in the same best known method (BKM) wet process that includes pre-clean, texturization, and final clean. Wafers were then processed for the standard PECVD process. As can be seen from Table 3, the efficiency averaged 18.87% and 18.43% for slurry and diamond-cut wafers, respectively while the control group wafers averaged 19.44%. The wet process conditions were different from the BKM, but the standard PECVD conditions were tuned.

Table 3: Un-optimized PECVD conditions.

Experiment	Wafer/Cell Parameters					
	Lifetime (µs)	Implied Voc (mV)	Efficiency (%)	Voc (mV)	Jsc (mA/cm^2)	FF (%)
Material A (slurry)	574	704	18.87	715.6	35.709	73.87
Material B (Diamond)	417	691	18.43	705.1	35.236	73.46
Control Group	897	727	19.44	716.8	36.05	75.25

Then, another set of wafers were run in which the PECVD parameters were tuned for these BKM wafers. The results are shown Table 4. Half of the wafers were run through another final clean step in HF/Rinse/Dry prior to the PECVD (Material A-1) and the efficiency was 19.98%. The other half (Material A-2) was processed through an SC1/SC2/HF sequence and the efficiency averaged 19.70%. Both materials A-1 and A-2 averaged higher than the control group's 19.68% average efficiency as shown in Table 4. This confirms once again that the PECVD process conditions must be tuned to the wet process conditions to achieve the highest possible efficiency. The fine tuning of the PECVD parameters could include for example, such parameters as the gas flow rate, film thickness and conformity at peaks and valley, plasma to condition the i-layer, dopant intensity, and annealing in vacuum.

Table 4: PECVD conditions optimized for the wet processes.

Experiment	Cell Parameters				
	Wet Process	Efficiency (%)	Voc (mV)	Jsc (mA/cm^2)	FF (%)
Material A-1	HF only	19.98	720	36.25	76.60
Material A-2	SC1-SC2-HF	19.70	716	37.62	73.16
Control Group	SC1-SC2	19.68	713	36.92	74.70

Conclusions

Results show that wafer quality plays a key role in the etch characteristics of Si wafers. Data also show that cleaning is required to normalize the surface of different wafers to render them nearly similar when introduced to the etch bath. Of equal importance is the final cleaning step in which the addition of an appropriate pyramid rounding step can further enhance the cell performance. At the same time, lowest metal signature on the wafers must be guaranteed by the advanced HF/HCl clean prior to the PECVD step. The data also highlight the importance of coupling the texturization and cleans with the PECVD process to obtain the highest possible cell performance. Uniform texturization and pyramid size yield higher current while good cleaning yields higher lifetime and hence voltage. The PECVD process has to be tuned and equally optimized so that the overall cell performance is maximized.

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