Using an ozonated-DI-water technology for photoresist removal

Jae-Inh Song, Richard Novak, Ismail Kashkoush, and Pieter Boelen, *Akrion*

An environmentally friendly alternative to sulfuric acid–based cleaning chemistries, DIO_3 processing can lower operating costs while minimizing defect densities and surface residues.

As the semiconductor industry shifts from 200- to 300-mm wafers, the use of ozonated deionized water (DIO_3) in surface cleaning processes is expected to become common. The technology, which has the potential to lower operating costs while maintaining process capabilities, has been widely studied, with particular emphasis on its application in photoresist removal after dry etching or ion implantation.[1–6]

Most photoresist removal procedures consist of a combination of plasma-induced dry ashing and wet chemical treatments. Problems associated with the dry ashing process include incomplete resist removal and undesired by-products caused by the reaction among the photoresist, oxidizing gas, and dry etch residue. However, an even greater concern is the undesirable effects on electrical properties, such as intrinsic total charge to breakdown (QBD) and electrical breakdown fields, that can be caused by plasma-induced damage to sub-0.18-µm devices with a gate oxide of <40 Å. In addition, the oxidation reaction that occurs between the etch residue and the oxidizer gas in the plasma chamber during dry ashing creates residue that is difficult to remove in subsequent wet cleans.

Traditional wet cleaning processes rely on a mixture of sulfuric acid and hydrogen peroxide (SPM) or sulfuric acid with ozone (SOM). Although these chemicals are highly effective, the operating costs for sulfuric-based processes are significant.[7] Vast amounts of DI water are consumed to rinse off residual sulfuric acid and unoxidized particulate matter from wafer and carrier surfaces during the wet cleaning process, and expenses are incurred both in obtaining the water and treating and disposing of postprocess wastewater. Other operating costs include the expenses involved in the storage, distribution, and treatment of sulfuric acid mixtures and in the frequent replacement of wet station components. Such components have limited life spans because of their

constant exposure to high process temperatures—generally >130°C—and the corrosive properties of the acid.

The use of a DIO_3 cleaning tool, such as that developed by Akrion (Allentown, PA), can offer several advantages over other photoresist removal procedures. Its adoption can simplify the stripping process by replacing two separate steps—dry ashing and wet cleaning—with one, and reduce operating costs by eliminating expensive, and environmentally unfriendly, sulfur-containing process chemicals. While minimizing defect densities and organic residue, the technology may also offer a smaller footprint than methods that require multiple process baths.

The DIO_3 Process

Unlike the SPM process, in which resist is undercut, floats away, and then is oxidized by hydrogen peroxide, the DIO_3 process directly oxidizes resist on the wafer surface. The resist becomes progressively thinner during this reaction, and the cleaning solution remains clear during the entire process. The chemical reaction that takes place during the DIO_3 process is

$$-CH_2^- + 3O_3 \rightarrow 3O_2 + CO_2 + H_2O$$

and the reactions in SPM processes are

$$H_2SO_4 + H_2O \rightarrow H_2SO_5 + H_2O$$

$$-CH_2 + 3H_2SO_5 \rightarrow 3H_2SO_4 + CO_2 + H_2O$$

Figure 1 depicts the two types of stripping procedures in simplified schematic drawings. In addition to directly oxidizing the resist, the oxidation reaction in DIO_3 processing between ozonated water and bare silicon induces the growth of a thin (~9.5-Å) oxide layer on the wafer surface. This chemically induced oxide minimizes particle additions because both the zeta potential on the silicon surface and the Van der Waals attractive force between the wafer and particles are reduced when the previously hydrophobic surface is rendered hydrophilic. The oxidation reaction also minimizes levels of total organic compounds.

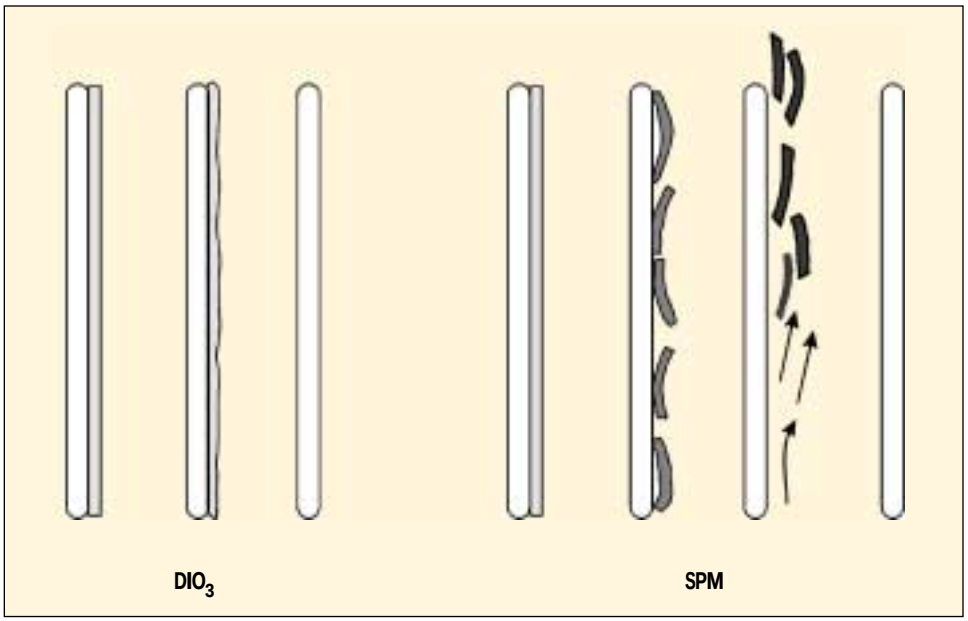

Figure 1: Simplified schematics of the DIO_3 and SPM photoresist stripping processes. In DIO_3 cleaning, resist is oxidized directly, whereas in SPM procedures, it is first undercut and then flows free of the wafer before oxidation.

The flow scheme in the DIO_3 immersion equipment is shown in Figure 2. In this system, ozone is produced from O_2 gas in an ozone generator and fed into a static mixer, where it is combined with DI water. This mixture is then fed into the bottom of the process bath. Gaseous ozone is also fed in a uniform stream to the bottom of the process bath via a specially designed diffusion device. The gaseous and dissolved ozone enter the bath simultaneously, and both are monitored using in-line analysis. With closed-loop recirculation, liquid flows from the process vessel to a pump, after which it flows through a heat exchanger, a sensor, and a filter back to the mixer. Finally it reenters the vessel. In this system, the dissolved ozone concentration stabilizes in the range of 10–50 ppm, depending on the process temperature (which can range from 18° to 50°C).

Process Optimization Studies

During the development of the DIO_3 system, a variety of tests were conducted to assess the technology's photoresist removal effectiveness.

Strip Rate. One set of tests assessed the effect of process temperature and ozone concentration on the average photoresist stripping rate. As the results in Figure 3 indicate, the stripping rate increased dramatically with an increase in the dissolved ozone concentration in the process bath. The data also show that the optimal baked-photoresist removal rate averaged 65 nm/min at ambient temperatures <40°C. This low-temperature capability greatly simplified equipment design and maintenance by eliminating the need for an upstream heater or heat exchanger. Strip-rate tests were run using many types of photoresist in addition to that used to achieve the results shown in Figure 3. The resists tested included AZ 1518, 7209, and 7220; HIPR 512; JSR 7158 and IX710; MCPRi 7010; PFX 15D1; PFI 26A, 26B, and 38A9; Shipley S1808 and S1813; and System 827

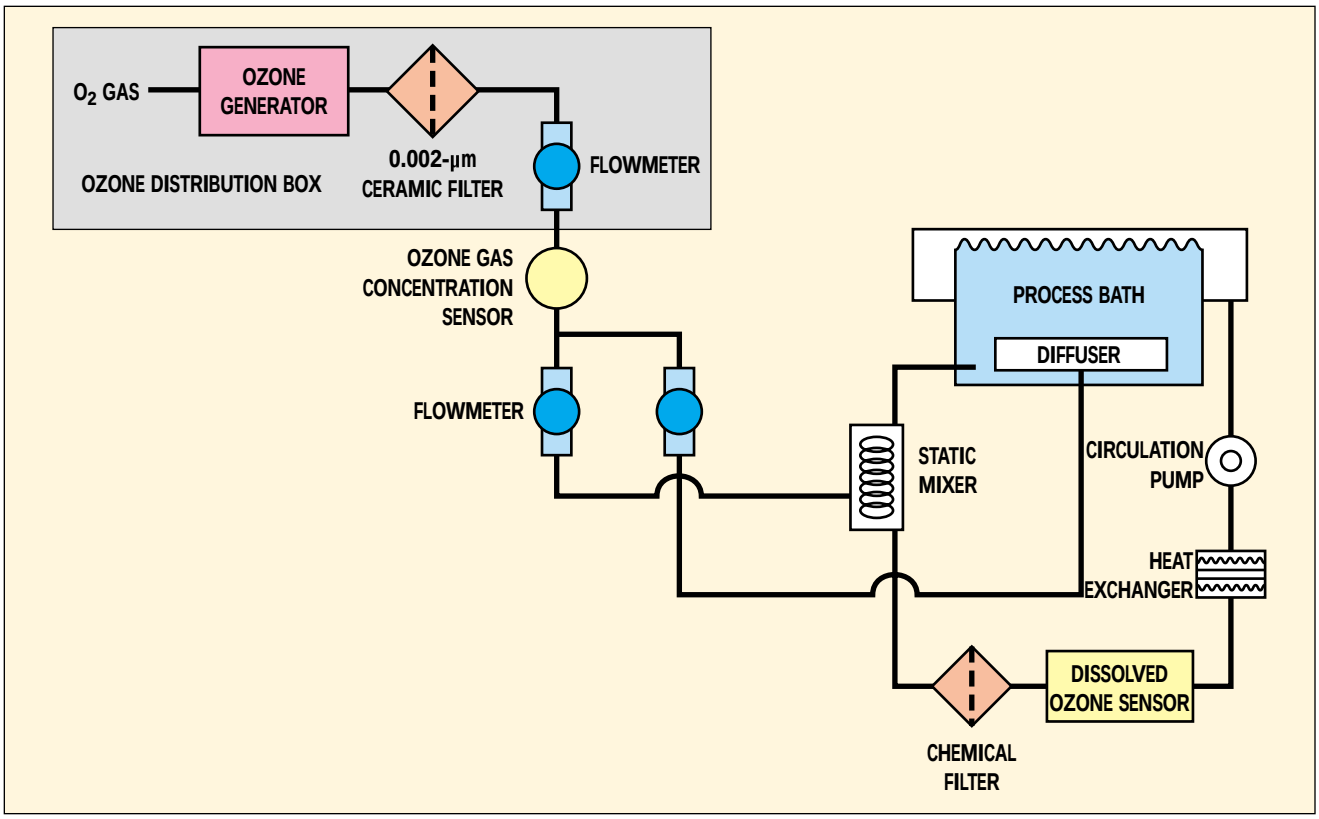

Figure 2: The flow scheme in the DIO_3 immersion tool.

THMR-ip 3300. It was found that the stripping rate does not depend on the resist type.

Although the removal rate achieved in this testing seems low compared to some previously published data from studies at subambient temperatures, it should not be a concern in future device manufacturing processes.[5] The photoresist thickness used in critical processes such as gate line, deep and small metal contact, and shallow trench isolation is expected to remain below 500 nm for sub-quarter-micron IC devices.

Microcontamination. In implementing the DIO_3 technology, the level of metal contaminants in the process bath was a major concern for several reasons. The process tool uses a metallic electrode to generate reactive ozone from oxygen, and it is known that metallic impurities have a tendency to adhere to hydrophobic surfaces after photoresist stripping. Minute amounts of such impurities can cause various defects, including silicide/silicate formation, gate oxide integrity failure, silicon surface pitting, and electrical current leakage in dielectrics in front-end processes. To address this concern, the metallic contamination contribution of the DIO_3 process was evaluated using vapor-phase decomposition total reflection x-ray fluorescence spectroscopy (VPD-TXRF). Comparative results for wafers processed by either DIO_3 or

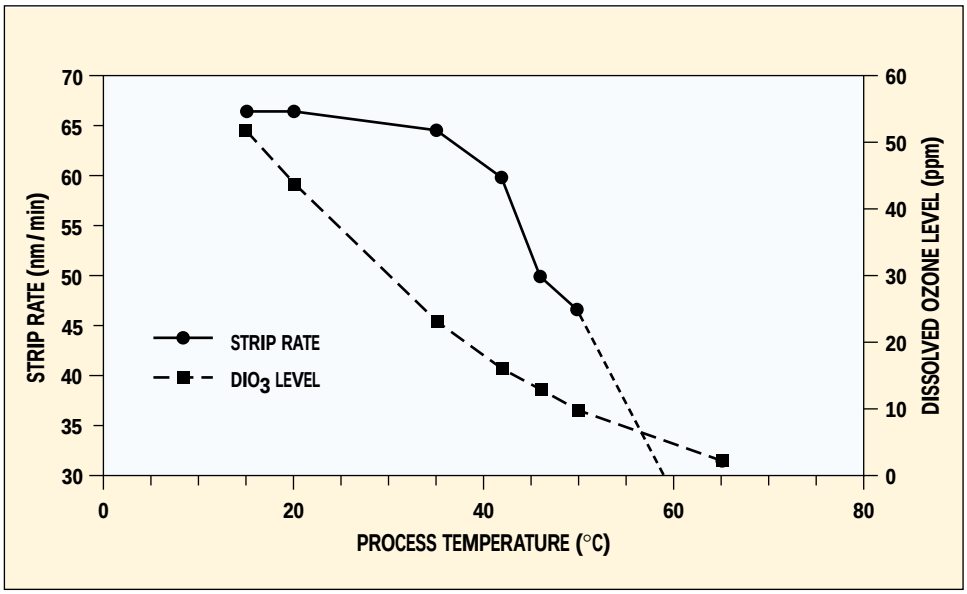

Figure 3: Data showing the effect of process temperature and dissolved ozone concentration on the average stripping rate of the DIO_3 process with a baked 1.3-µm photoresist. The optimal removal rate averaged 65 nm/min.

Process Type	Metallic Contaminant (10^{10} atoms/cm^2)														
	S	Cl	K	Ca	Ti	Cr	Mn	Fe	Co	Ni	Cu	Zn	As	Br	Pb
SPM	750	5.6	75	2.3	< DL	0.18	< DL	0.92	0.05	0.18	0.03	0.98	< DL	0.9	0.02
DIO_3	52	20	3.1	0.5	0.6	< DL	0.05	0.66	< DL	0.18	0.03	0.42	0.12	0.86	0.039
Reference wafer (unprocessed)	82	40	< DL	0.6	< DL	< DL	< DL	0.09	< DL	0.02	0.06	0.05	0.02	0.39	0.005
Detection limit (DL)	3.5	0.6	0.8	0.3	0.2	0.07	0.048	0.04	0.03	0.02	0.02	0.02	0.01	0.01	0.005

Table I: Metallic contamination levels measured using VPD-TXRF on a reference wafer and following resist stripping with either an SPM or DIO_3 technology. The measurement instrument's detection levels for each metal are also listed.

SPM are presented in Table I. As these data indicate, no significant metallic contamination was observed on wafers processed with DIO_3. In addition, sulfur contamination, a significant cause of wafer surface hazing associated with SPM processing, was not observed following the ozonated-water process. It is believed that DIO_3 eliminates ionized metallic impurities from the wafer surface via the oxidation reaction of the highly reactive ozone radical (O_3^+).

The stripping rate increased dramatically with an increase in the dissolved ozone concentration in the DIO_3 process bath.

In a typical manufacturing environment, the SPM photoresist stripping process sequence includes RCA standard cleans 1 and 2 (SC-1 and SC-2). The SC-2 clean, which consists of hydrochloric acid (HCl) and hydrogen peroxide, is used to remove metallic residues such as iron and zinc, which are often deposited during the SC-1 step. With DIO_3 processing, injecting a small amount of HCl into the process water or the postprocess rinsewater effectively removes such trace metals from the wafer surface, eliminating the need for the SC-2 step and thereby lowering overall operating costs.

The possibility of eliminating the SC-1 step following the DIO_3 process was also investigated. In that study, surface particles ≥0.16 µm were measured with a Surfscan 6200 (KLA-Tencor, San Jose). As shown in Table II, the final particle counts following a DIO_3/SC-1/rinse/dry sequence were lower than those obtained following DIO_3/rinse/dry or DIO_3/dry sequences. Compared to the DIO_3/rinse/dry results, the counts were approximately 25% lower when the SC-1 step was included.

On certain highly implanted wafers, where the photoresist is used as a blocking layer to form a shallow junction (for source and drain) after gate etch, it is desirable to combine dry ash and wet chemical stripping processes. In such cases, SPM followed by SC-1 is the usual post-dry-ashing wafer cleaning sequence. The role of SPM is to remove by-products that are formed during the reaction between

Run Number	DIO_3/SC-1/Rinse/Dry	DIO_3/Rinse/Dry	DIO_3/Dry
1	90	65	162
2	70	111	152
3	75	127	139
4	71	101	142
5	79	107	121
6	73	102	113
7	62	109	121
8	79	109	143
9	87	87	165
10	73	99	132
Average	76	102	139

Table II: Total particle counts at ≥0.16 µm on unashed wafer surfaces following various DIO_3 process sequences.

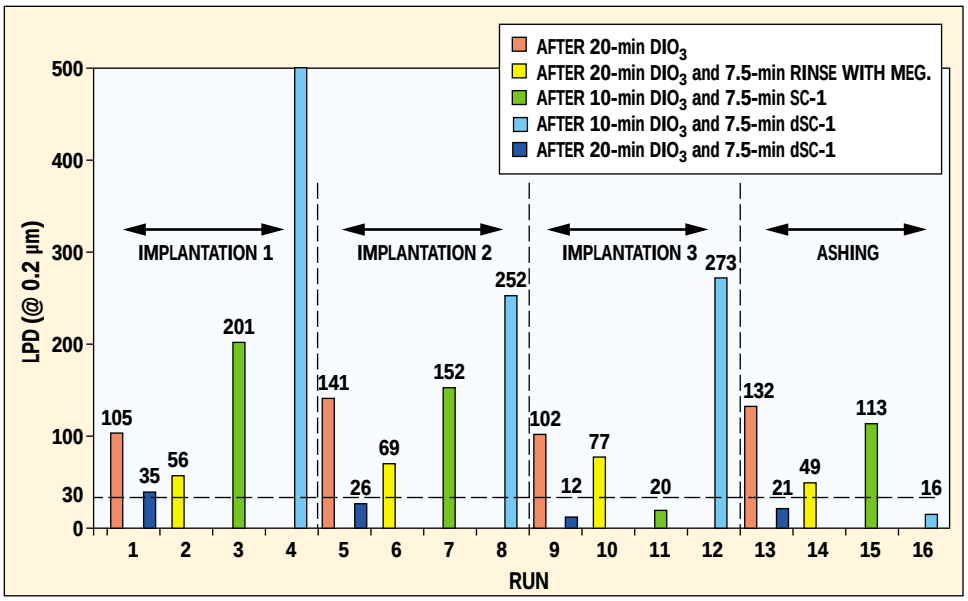

Figure 4: Light-point defect (LPD) measurements indicating the efficiency of DIO_3 alone and combined DIO_3 and SC-1 processes for post-dry-ashing wafer cleaning.

photoresist and the reactive gas in the ashing chamber. To investigate the use of ozonated water rather than SPM in this postash cleaning step, light-point defect measurements were taken on wafers that had been treated using various process sequences. As shown in Figure 4, the DIO_3-only treatment was not sufficient to obtain good defect counts; however, the combined DIO_3 and SC-1 process sequences yielded satisfactory to excellent results, particularly when a 20-minute DIO_3 immersion was used.

The Recommended Process. Based on the studies discussed above and assuming a common device structure of <12,000 Å, the recommended process sequence for photoresist removal with DIO_3 is as follows:

1. A 15–20-minute immersion in the DIO_3 process bath at ambient temperature to remove photoresist.
2. SC-1 processing for 7–10 minutes at 50°C with megasonics to remove particles and light organics.
3. A 7–10-minute cascade-type DI rinse at ambient temperature to rinse off the SC-1 chemistry and cool the wafers.
4. An 8.5-minute cycle in a dryer to remove rinsewater from the wafers.

As the micrographs in Figure 5 indicate, this DIO_3/SC-1/rinse/dry sequence thoroughly removes the photoresist from a patterned wafer. (Before undergoing the DIO_3 process, the wafer shown had a 1.05-µm-thick HipR 6512 resist layer hard baked at 100°C.)

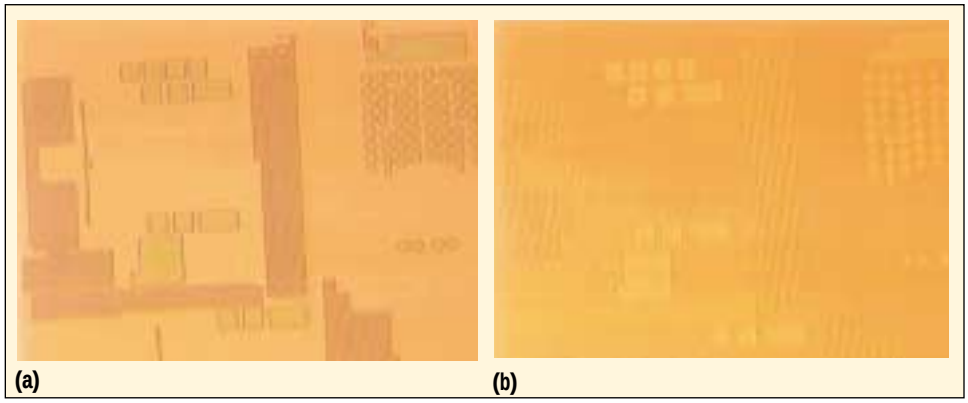

Figure 5: Micrographs (100×) of a patterned wafer before (a) and after (b) DIO_3 processing, showing that photoresist had been removed effectively.

Electrical Performance and Yield

In another study (the results of which are presented in Figure 6), researchers investigated the effect of DIO_3 processing on device properties and yield.[8] In that work, the intrinsic breakdown of thin oxide on simple gate modules was measured on wafers cleaned with either a DIO_3 or SPM process followed by standard cleans SC-1 and SC-2. The gate oxide layer was 120 Å thick. These measurements indicated that the probability of intrinsic QBD failure—which may result from defects caused by such contaminants as particles, organic residue, and metallic impurities—did not differ significantly for wafers cleaned with the two processes. Yield loss for wafers processed using DIO_3 was also comparable to that for wafers cleaned with SPM.

Conclusion

Studies have shown that DIO_3 is a viable substitute for sulfuric acid mixtures in semiconductor resist stripping processes. When followed by an SC-1 clean, DIO_3 processing minimizes metallic contamination and particle addition on the wafer surface. The technology is also environmentally friendly and reduces operating costs because it eliminates the use of corrosive chemicals. More importantly, neither electrical device characteristics nor overall production yields are negatively affected by using the DIO_3 process.

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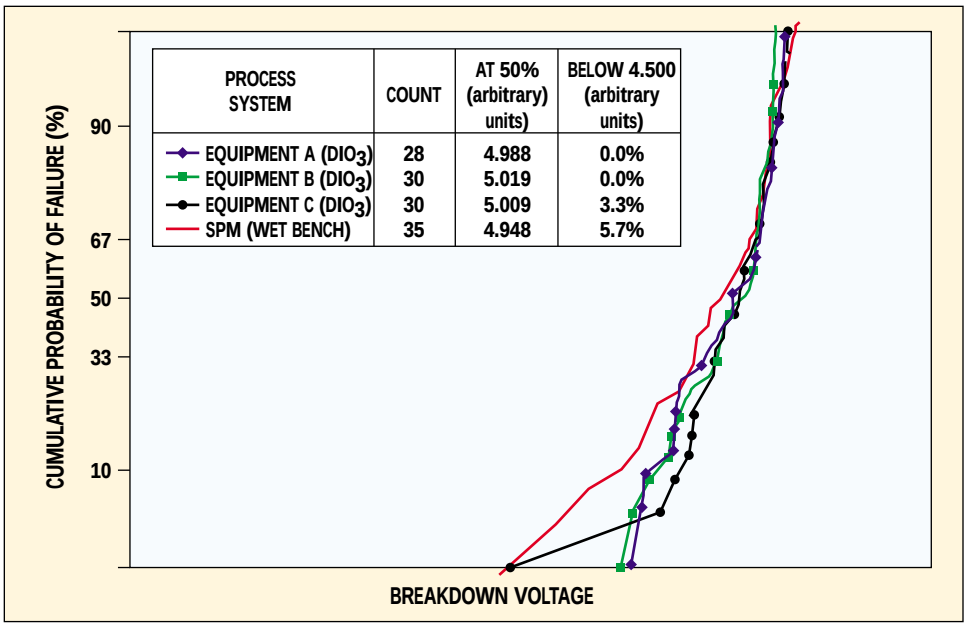

Figure 6: Cumulative failure of intrinsic total charge to breakdown.

of IMEC for sharing valuable information regarding the effects of DIO_3 processes on electrical properties and device yields.

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Jae-Inh Song, PhD, is vice president of process applications at Akrion in Allentown, PA. Before assuming this position, he served as manager of the cleaning and CMP process development team at Samsung's semiconductor R&D center. Song's main interests include manufacturing-oriented surface preparation and characterization technology, and yield enhancement via implementation of cleaning technology. He has authored or coauthored more than 30 journal publications and 40 conference presentations. He is also the holder or coholder of approximately 100 semiconductor process and equipment–related patents. He received a PhD in solution chemistry in 1989 from the University of Glasgow, UK. (Song can be reached at 610/530-3607 or jaeinh@compuserve.com.)

Richard Novak, PhD, is vice president of advanced technology and chief technical officer at Akrion. He previously served as a member of the technical staff at RCA Laboratories and has more than 25 years of experience in the semiconductor industry. He also cochaired the first four International Symposia on Wafer Cleaning. Novak received his PhD in ceramic engineering from the University of Illinois (Champaign-Urbana) in 1972. (Novak can be reached at 610/530-3449 or richnovak @aol.com.)

Ismail Kashkoush, PhD, is director of applications and process engineering at Akrion, where he is responsible for process R&D in the company's Class 1 applications laboratory. Specializing in microcontamination characterization, removal, and control, Kashkoush has published more than 50 articles in the area of wafer surface preparation. He received his PhD in engineering sciences from Clarkson University (Potsdam, NY) in 1993. (Kashkoush can be reached at 610/530-3379 or kashkoush@aol.com.)

Pieter Boelen is manager of European process support and applications for Akrion in Grenoble, France. He is responsible for a process research project at the Laboratory of Electronics, Technology, and Instrumentation (LETI) and customer application support in Europe. Boelen has authored or coauthored several publications in the area of wafer cleaning and surface preparation. He holds a degree in electronics engineering. (Boelen can be reached at +33 4 76884006 or pieter_boelen@compuserve.com.) M