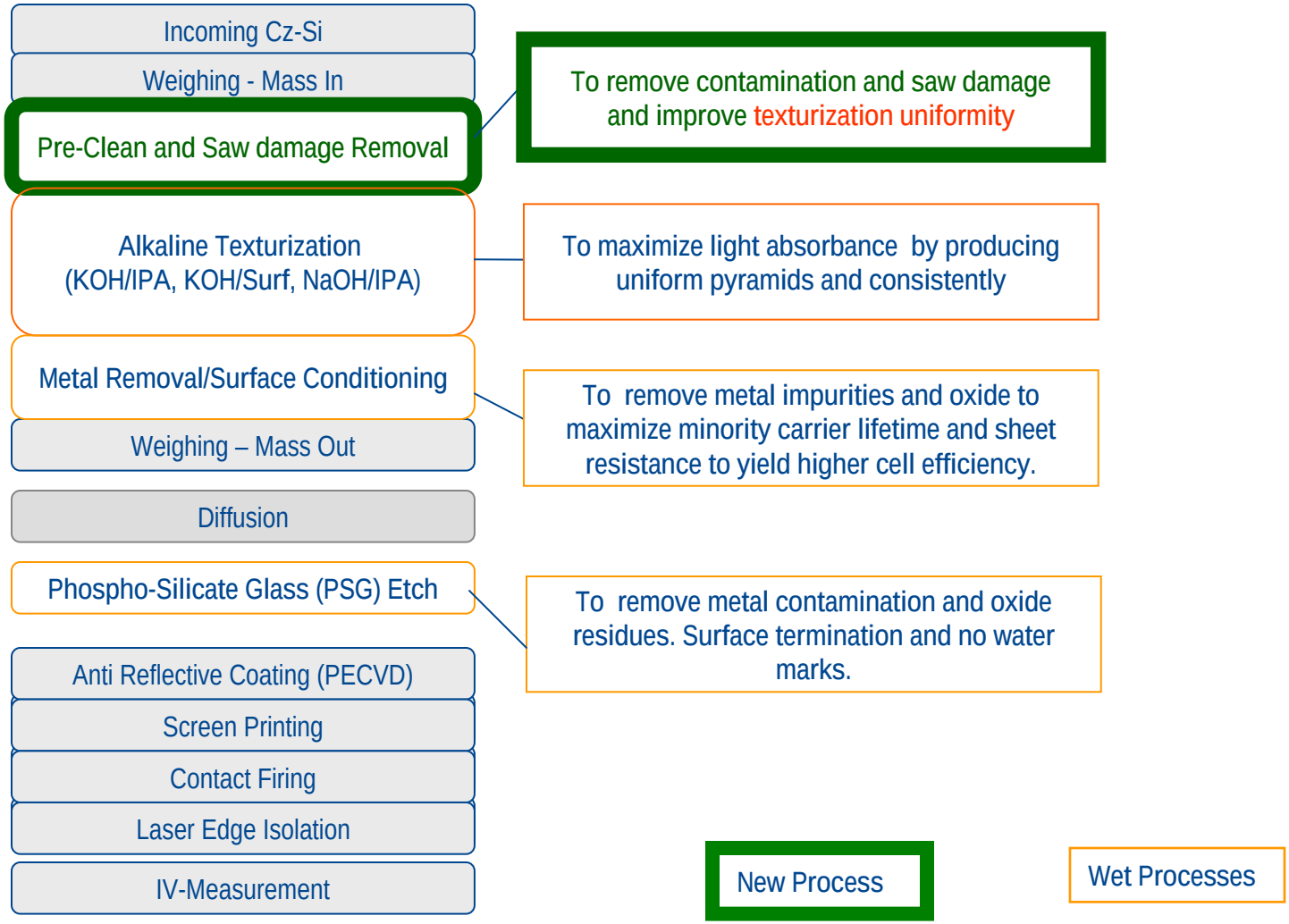
Wet Surface Conditioning of Monocrystalline Silicon Prior to Alkaline Texturization

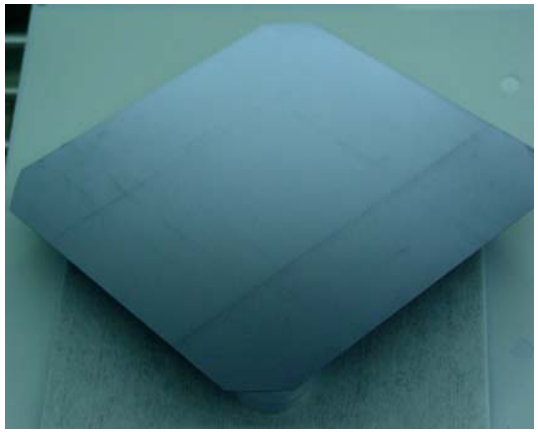
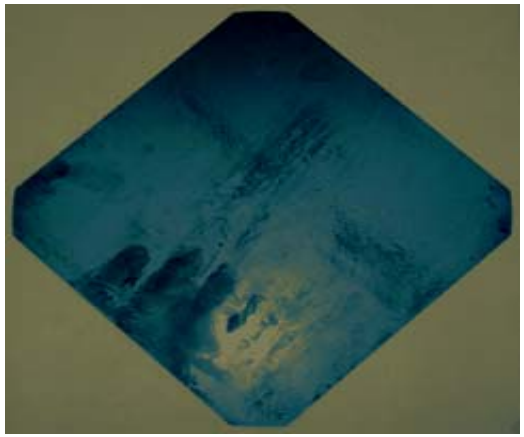
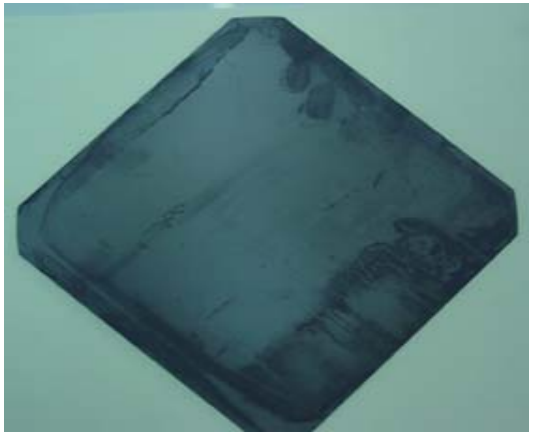
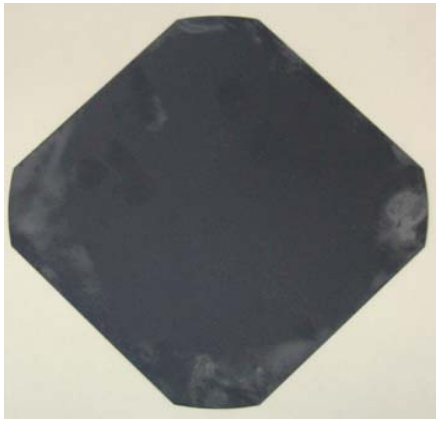
Presented at the 25th European Photovoltaic Solar Energy Conference and Exhibition, Sept. 6-10, 2010

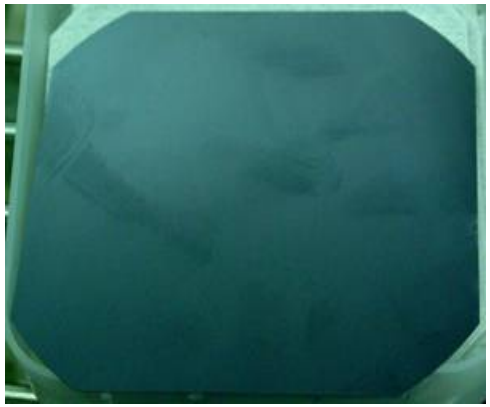
Ismail Kashkoush, PhD & Gim Chen, PhD

Objective and Process Flow



Typical Surface Contamination on Texturized Wafers

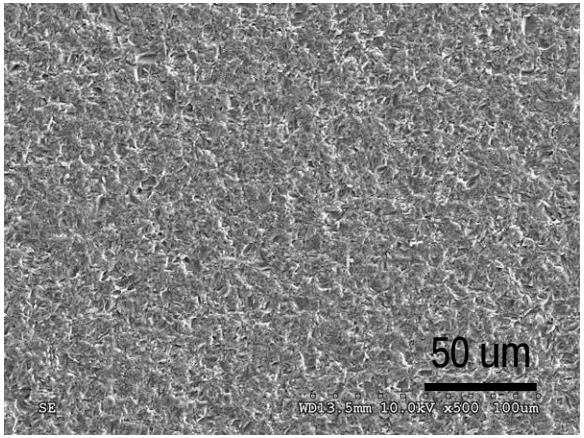


Applying a cleaning step prior to texturization is now needed

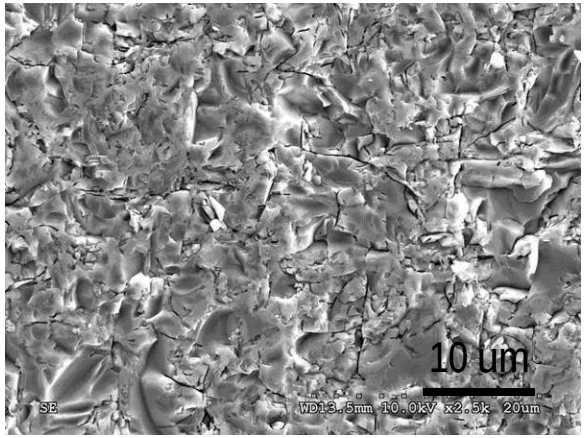
Experimental Conditions

Materials	125mm or 156mm c-Si solar wafers with <100> orientation from various suppliers
Wet Station	Akrion Systems GAMA 1098 wet station in Applications Lab
Chemical Processes	Recirculated bath for various time, followed by DI water rinse and dry; In split-lot tests, wafers receiving same chemical processes were run together • Pre-texture cleaning/etching: HF, KOH, APM, KPM, HF/HNO3, or combinations • Texturization and post-clean: KOH+IPA and HF/HCl (using a fixed BKM condition)
Weight Loss Measurement	Microbalance with a stagnant airflow chamber; digital display down to 0.0001 grams but resolution accuracy at 1 milligram
Silicon Removal Estimation	Formula: (weight-loss ÷ initial-weight) × initial wafer thickness
Reflectance Measurement	Ocean Optics HR4000CG spectrometer with integrating sphere

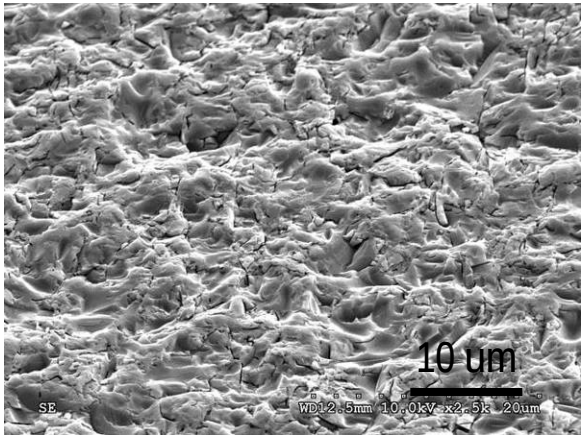
Typical Surface Morphologies



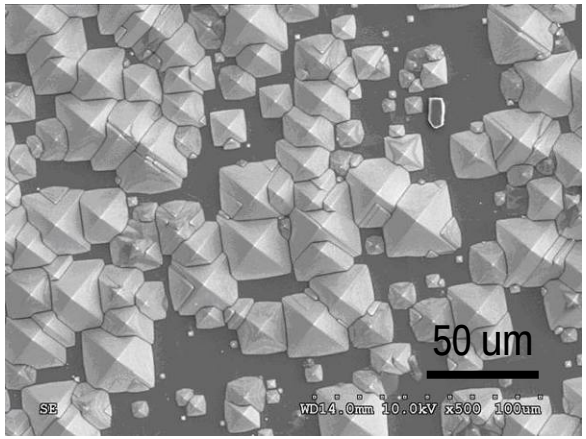
As-cut Surface (topdown 500X)



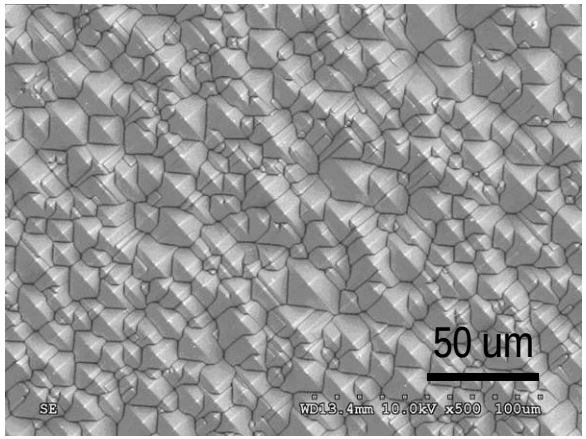
As-cut Surface (topdown 2500X)



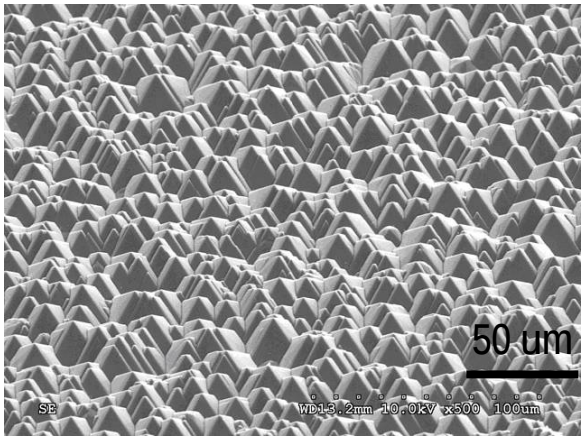
As-cut Surface (45° tilted 2500X)



Partially Textured Surface (topdown 500X)



Fully Textured Surface (topdown 500X)

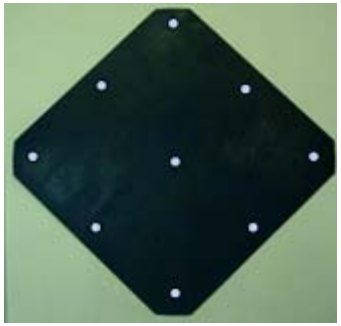


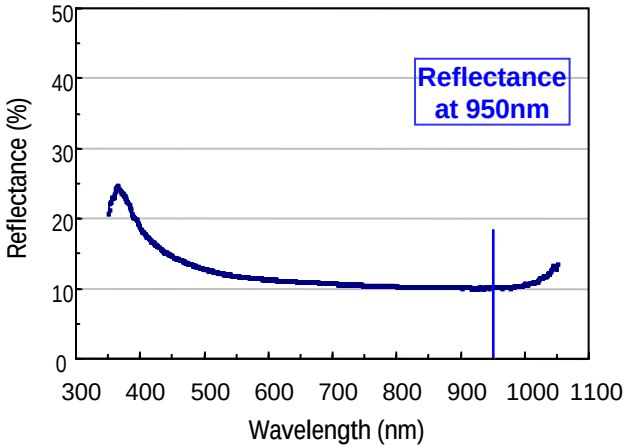
Fully Textured Surface (60° tilted 500X)

Effects of Pre-Cleaning on Reflectance
(wafers from the same supplier)

Sample	Process			Rfl% (Avg) @ 950 nm	Rfl% (Stdev) @ 950 nm
	Pre-Clean	HF Dip	Texturization + post-clean		
A-21	APM	Applied	BKM	9.22	0.10
A-22				9.47	0.11
A-23		Not Applied		9.41	0.07
A-24				9.50	0.21
A-27	KPM-1	Applied		9.42	0.15
A-28				9.18	0.10
A-29		Not Applied		9.18	0.14
A-30				9.31	0.13
A-33	KPM-2	Applied		9.34	0.10
A-34				9.46	0.09
A-35		Not Applied		9.39	0.13
A-36				9.36	0.12
A-39	Not Applied	Applied		9.05	0.10
A-40				9.05	0.29
A-41		Not Applied		9.07	0.32
A-42				9.10	0.13

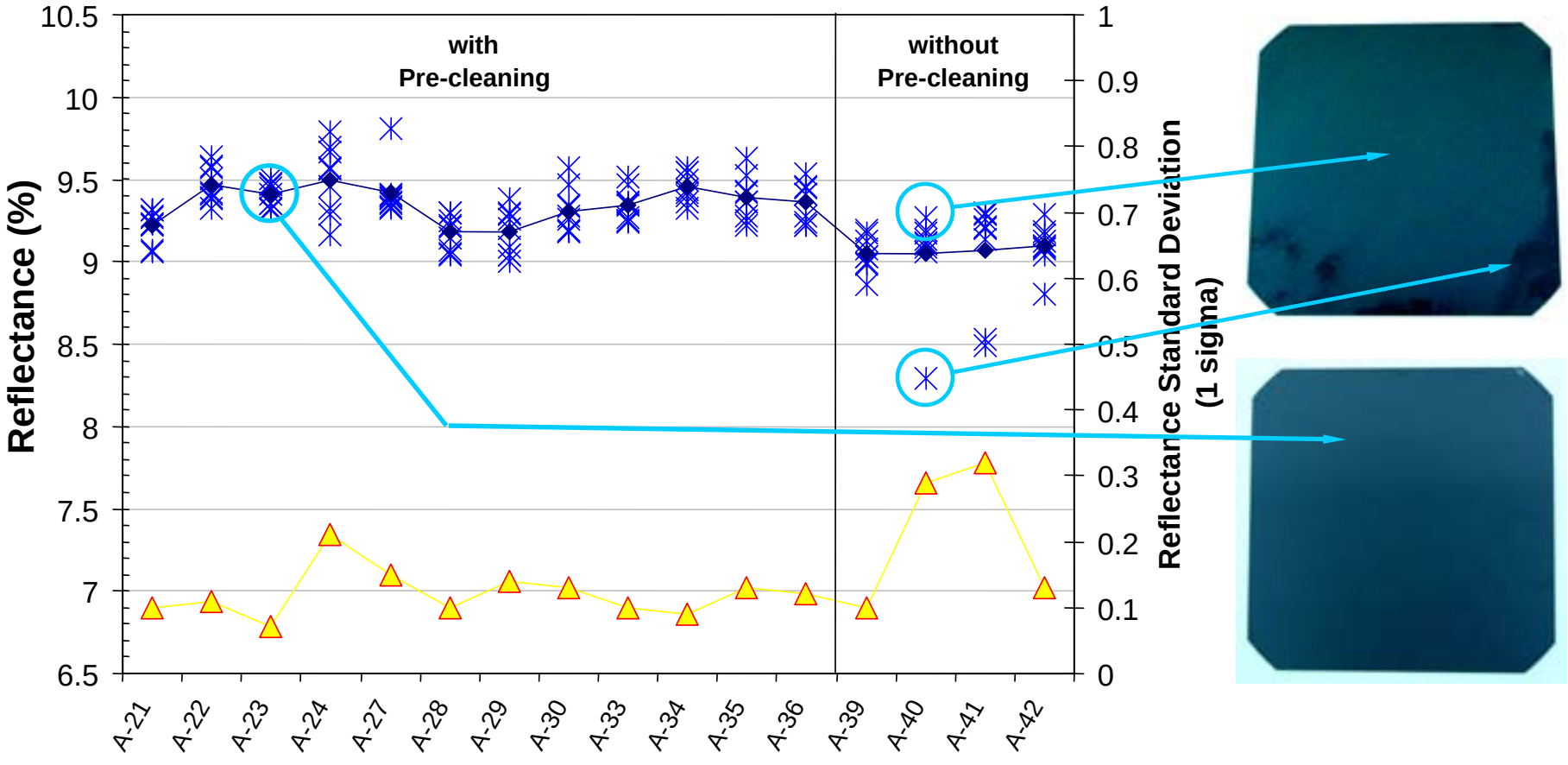
- Contaminated areas could be random and not on measurement spots
- Si etch rate in chemicals: KPM-1 > KPM-2 > APM > HF (near to zero)
- HF dip prior to texturization did not show significant effects on results





9-point Measurement per Wafer and representative reflectance spectrum for a spot

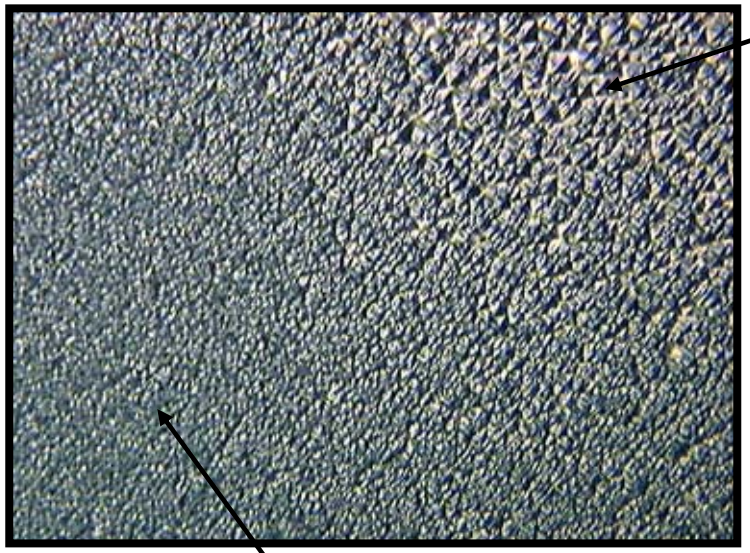
Reflectance Non-Uniformity by Surface Contamination (1)

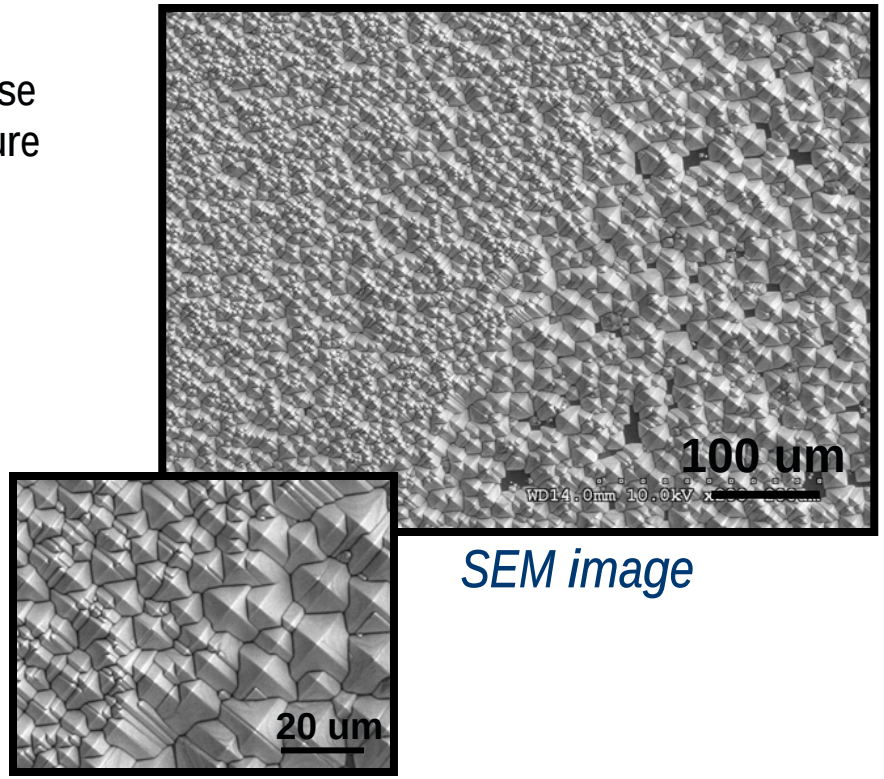


Pre-cleaning can reduce reflectance non-uniformity by removing surface contaminants

Texture Morphology of Contaminated Area (1)

Optical image (200X)

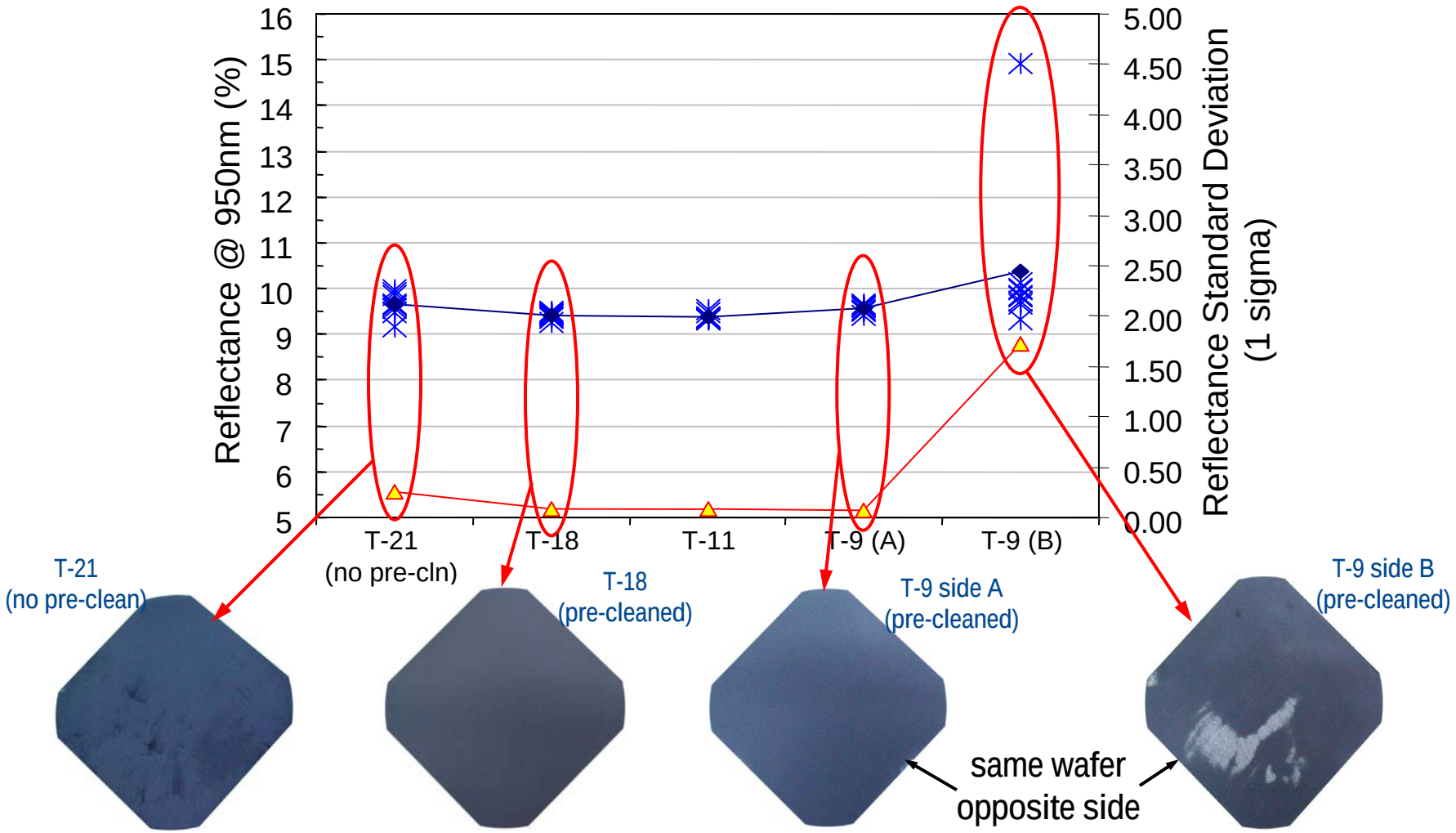




SEM image

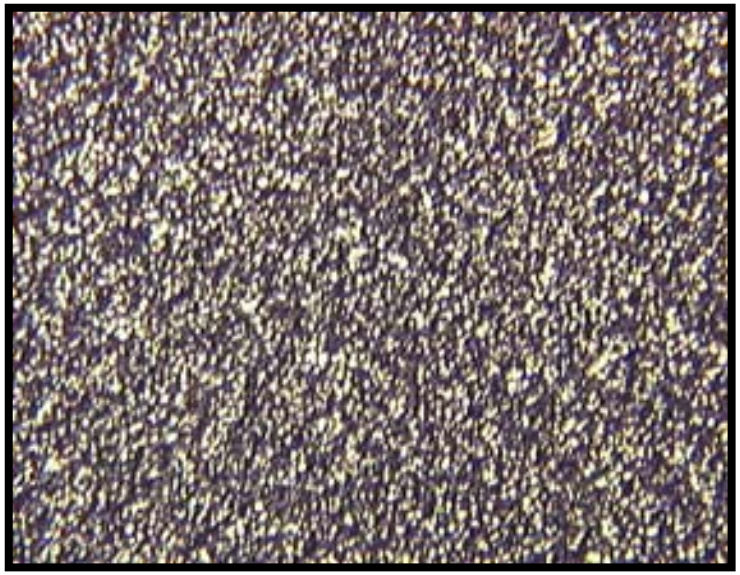
- Contaminated areas induce smaller pyramids
- Areas with smaller pyramids show lower reflectance

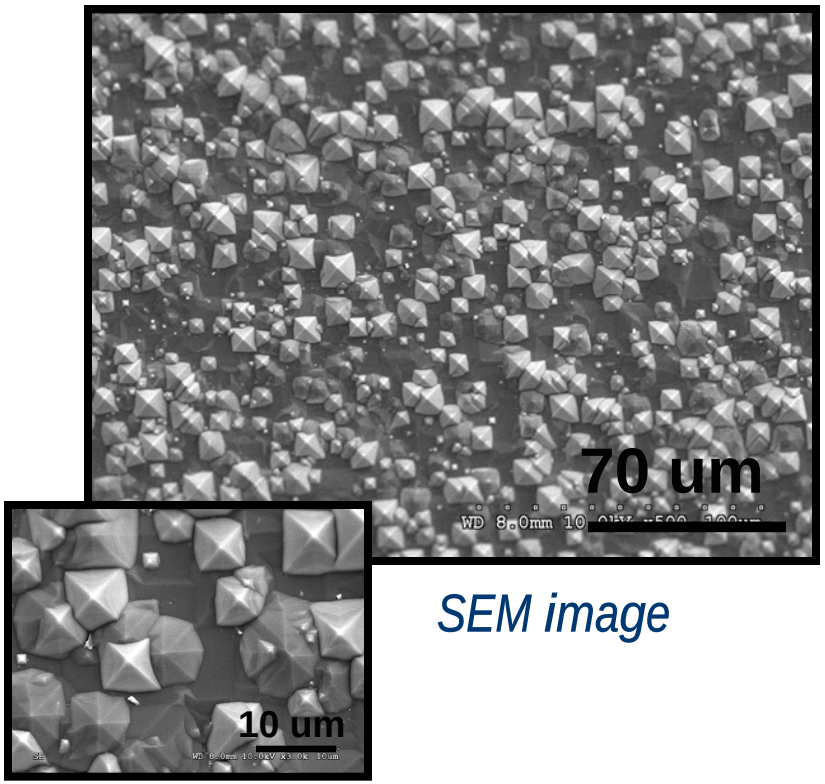
Reflectance Non-Uniformity by Surface Contamination (2)



Texture Morphology of Contaminated Area (2)

Optical image (200X)

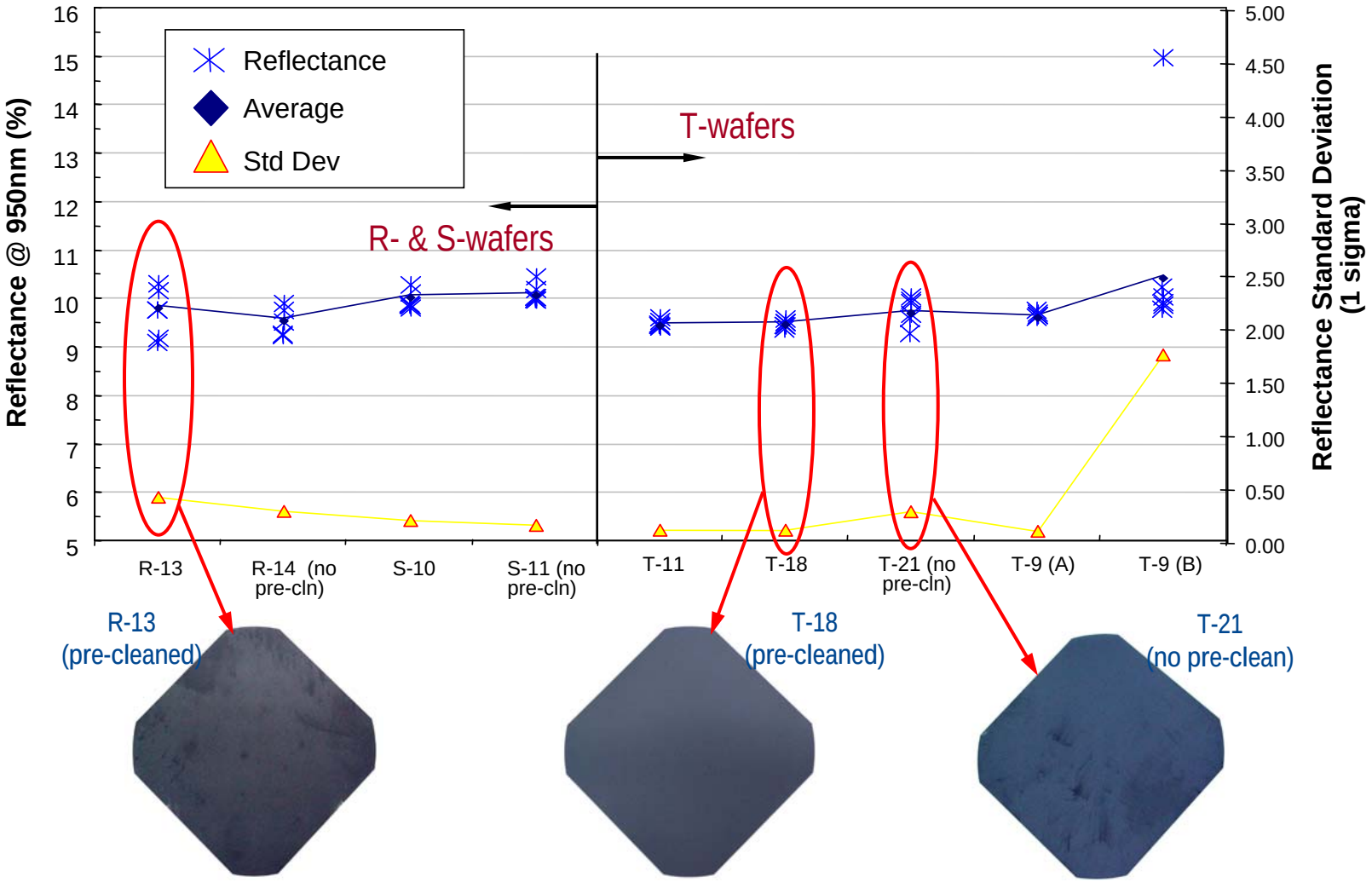




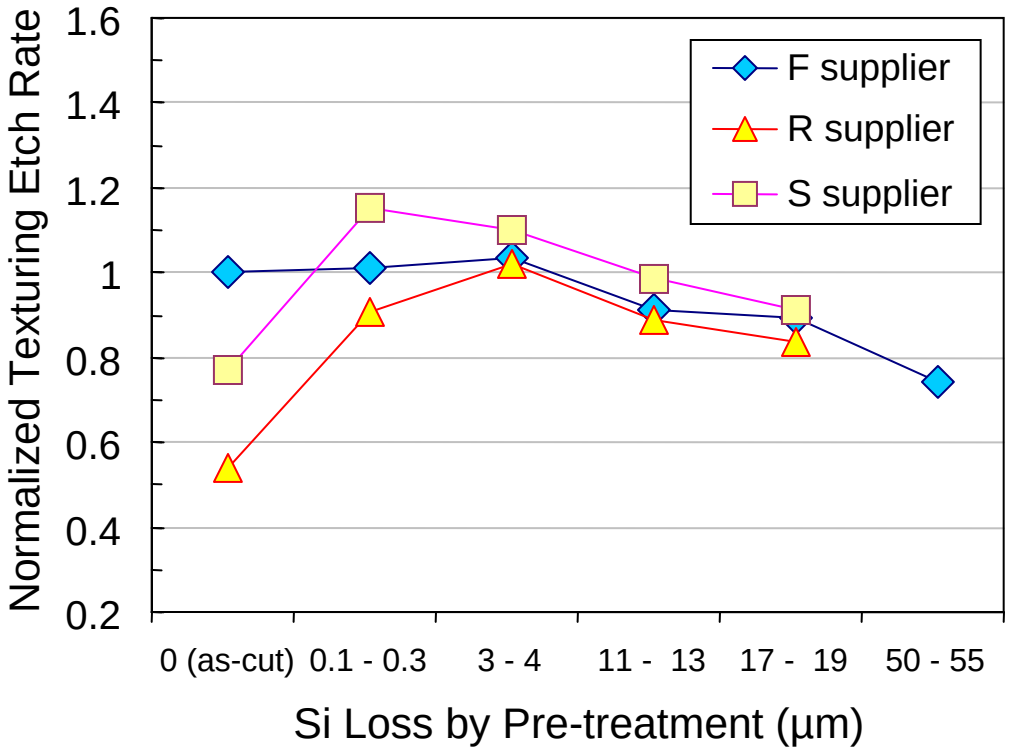
SEM image

- Contamination induces premature pyramid formation
- Areas with premature pyramids show high reflectance

Effect of Wafer Source on Texturization
(wafers from different suppliers)

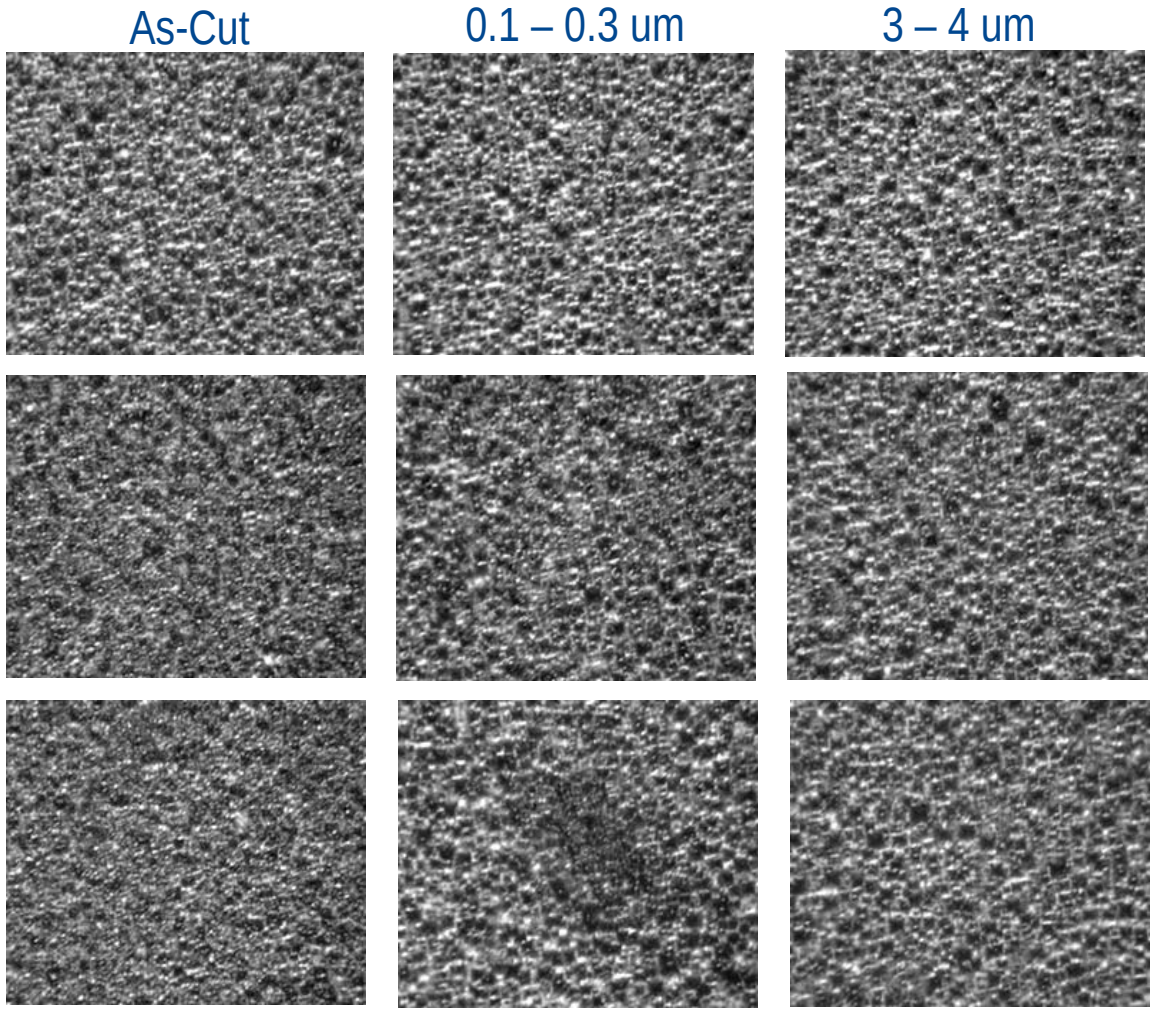


Texturing Etch Rates vs Pre-treatment with Different Levels of Silicon Removal



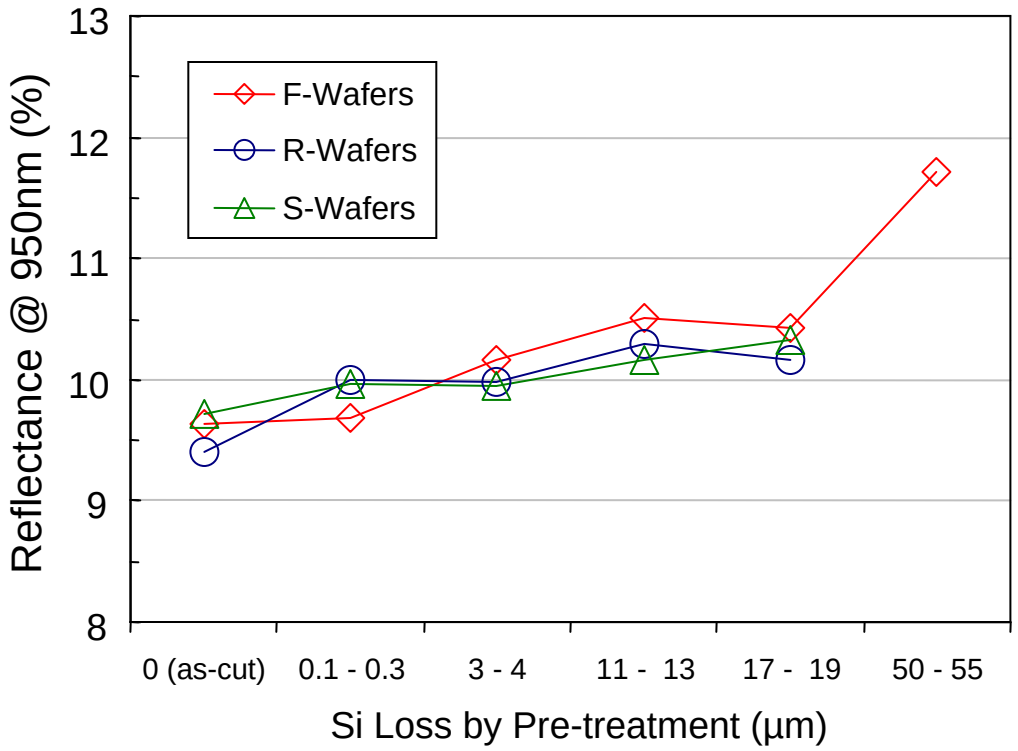
- F-wafers (like T-wafers) showed consistent texturing etch rates with or without pre-treatments, indicating mostly superficial contamination on wafer surfaces
- By removing > 1 um damaged layer, all three wafers showed consistent etch rates

Textured Images of Different Wafers vs the Level of Si Removal by Pre-treatment



More consistent surface texture between wafers of different sources after 3 – 4 µm Si removal by pre-treatments

Texture Reflectance vs Pre-treatment with Different Levels of Silicon Removal



Overall texture reflectance increases with the extent of silicon etch by pre-treatment

Summary

- With uncontrolled variables in manufacturing and handling, incoming solar wafers are subjected to various surface contaminations and need proper pre-cleaning treatments to yield consistent texturization results
- Surface contaminations can lead to dense/small and premature pyramid formation, causing relatively low and high reflectance, respectively (i.e. reflectance non-uniformity)
- Normal alkaline cleaning conditions used in semiconductor industry may not work effectively to remove all varieties of surface contaminations (i.e. < 0.5μm Si removal).
- More aggressive Si removal (> 1~2 μm) seems to be required for a more robust cleaning process
- Overdoing of the cleaning/etching may not be able to produce an optimal texturization result and can lead to other undesired effects (such as material loss, wafer flatness, etc.)