Simultaneous Removal of Particles from Front and Back Sides by A Single Wafer Backside Megasonic System

Chan Geun PARK[1, a] and Hong Seong SOHN[1,b]

[1]Akrion Systems LLC, 6330 Hedgewood Drive, Suite #150, Allentown, PA 18106, USA

[a]cpark@akrionsystems.com, [b]seasunfa@akrionsystems.com

Keywords: backside megasonic, backside clean, particle removal efficiency.

Introduction

In IC manufacturing, particle removal from a wafer's back side (BS) has become as important as that from the front side (FS). For example, during lithography, BS particles can cause a variation on the topside surface topography. This may result in a focus-spot failure due to the reduced process window for depth of focus (DOF) as shown in Fig. 1. This problem increases as the feature size decreases. BS particles may cause other problems in wet benches, where BS particles can be transferred to the adjacent front side of wafers. Fig. 2 shows these FS particles, which usually appear as flow or streak patterns on the wafer [1].

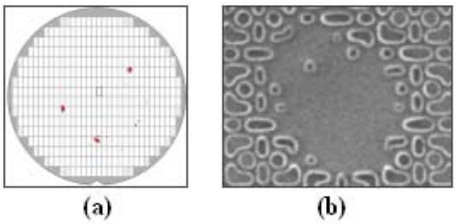


Fig. 1 Impact of BS particles on FS patterning: (a) map of pattern defectivity and (b) SEM image of these pattern defects

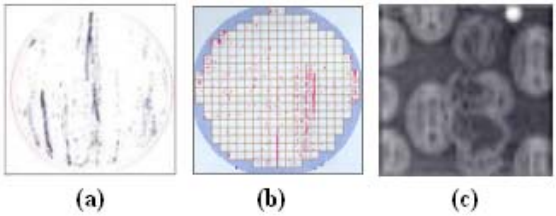


Fig. 2 Typical flow type defects caused by the particle transfer from BS to FS in a wet bench; (a) streaks on (a) bare silicon wafer, (b) patterned wafer and (c) its SEM image

The typical source of BS particles is wafer handling with either an electrostatic or vacuum chuck or from plates and stages in the vacuum chamber which result in defect maps as shown in Fig. 3. For pre-lithography BS particle cleans, these particles are generated mainly during dielectric deposition, metal sputtering or implant/ash.

Because of the typical elevated temperature in the vacuum process, particles can adhere strongly to the wafer backside. Compounding the issue, the introduction of immersion lithography for advanced device fabrication brings increased concern about the presence of loose films and particles that can accumulate at the wafer edge (bevel and apex). The wafer undergoes multiple wafer processing steps in the device flow and contamination can be introduced at each step. Because of the high throughput requirements for scanners, the immersion hood water layer moves at speeds of about 0.5m/second and this exerts high capillary forces from the trailing edge of the water meniscus that can dislodge defects from the

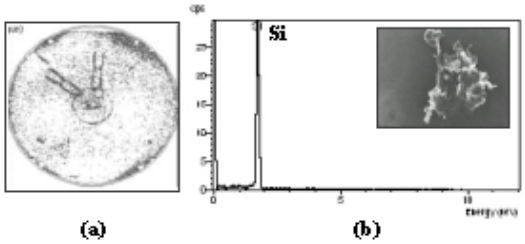


Fig. 3 Typical BS particles generated during a vacuum process; (a) BS particle map after CVD and (b) SEM image and its EDX analysis spectrum of BS particulates

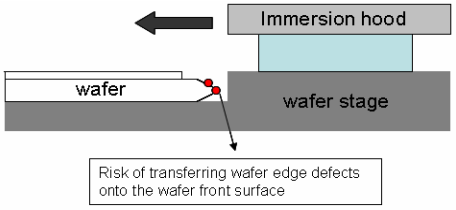


Fig. 4 Wafer edge defect migration concern at immersion lithography process

edge and re-deposit them on the front side of the wafer as shown in Fig. 4. [2] While the critical particle size for BS is larger than FS, it tends to decrease as the feature size decreases as indicated by Table I. [3]

Table 1. Particle size requirements from ITRS 2008

Year of Production	2007	2008	2009	2010	2011	2012	2013
DRAM ½ Pitch (nm)	68	59	52	45	40	36	32
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	68	59	52	45	40	36	32
Wafer edge exclusion (mm)	2	2	2	2	2	2	2
Critical particle diameter, d_c (nm)	34.1	29.7	25.8	22.5	20.0	17.9	15.9
Critical particle count, D_{pw} (#/wafer)	65.1	65.1	65.1	65.1	65.1	269.4	169.7
Back surface particle diameter: lithography and measurement tools (µm)	0.12	0.12	0.1	0.1	0.1	0.1	NA
Back surface particles: lithography and measurement tools (#/wafer)	200	200	200	200	200	200	NA
Back surface particle diameter: all other tools (µm)	0.16	0.16	0.14	0.14	0.14	0.14	NA
Back surface particles: all other tools (#/wafer)	200	200	200	200	200	200	NA

So far most silicon wafer cleaning tools have been developed in order to remove FS particles by physical force and/or chemical reaction. Whenever BS cleans are needed, wafers are flipped over before and after cleaning or cleaned by indirect physical force transmitted through the wafer with chemicals dispensed to the back side of the wafer. But, in these cases, BS particle removal efficiency (PRE) is much lower than FS PRE. In this paper a new single wafer megasonic system was introduced and both FS and BS PREs were evaluated as a function of megasonic power/time and source of contamination.

Experimental

Experiments were performed on a 300mm Akrion Systems Goldfinger® Velocity™ tool. Megasonic sound energy is delivered to the wafer back side directly through a plastic-covered piezoelectric material to a liquid meniscus pathway provided by the BS megasonic system (BS Meg) installed beneath the wafer. The picture of the BS Meg-meniscus between BS Meg and wafer back side and the sound transmission schematic are shown in Fig. 5.

For the particle removal experiments, 300mm bare silicon wafers were contaminated with Si_3N_4 particles (200nm in diameter and around 20,000 particles per wafer) or in a metal sputtering chamber after the wafer was flipped. The number of particles on the wafer was counted from 65nm-size by SP2 (KLA-Tencor) before and after contamination and after cleans.

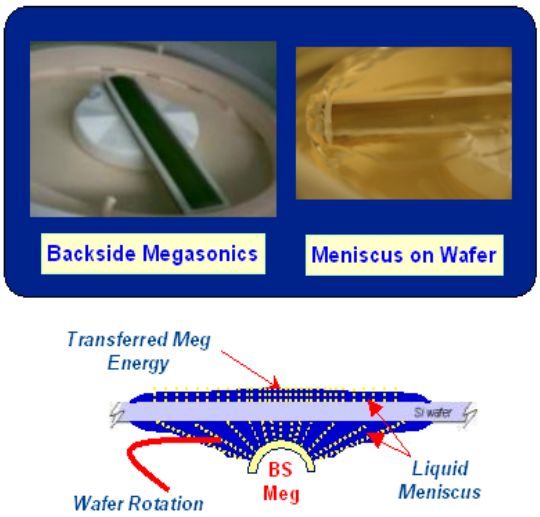


Fig. 5 GoldFinger BS Megasonic system and its schematic diagram of the sound transmission path

Results and Discussions

Front and back side particle removal efficiencies for Si_3N_4 particles were evaluated as a function of BS Meg power and time by dispensing dilute SC1 to wafers. Fig. 6 shows that back side PRE with the BS Meg and SC1 already reached >85% at 70W and 30 second condition, Back side PRE by BS Meg was almost 7 times higher than BS PRE of the Goldfinger® front side megasonic system (FS Meg). Front side PRE was comparable using either megasonic as shown in Fig. 7. This indicates that the BS Meg is able to remove particles from both

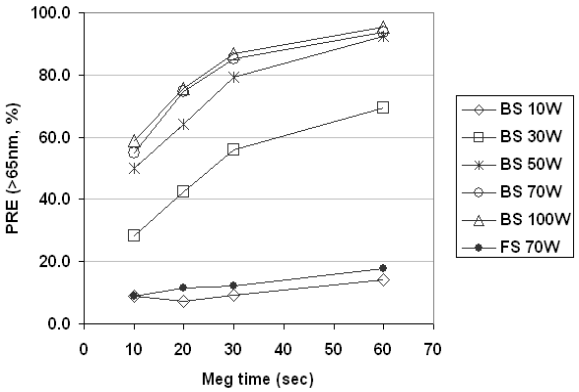


Fig. 6 Backside (BS) PRE in SC1 as functions of BS Meg power and time

the front and back sides at the same time with sufficiently high PRE.

Figure 8 shows results of PRE testing for the difficult removal of Electrostatic Chuck (ESC)

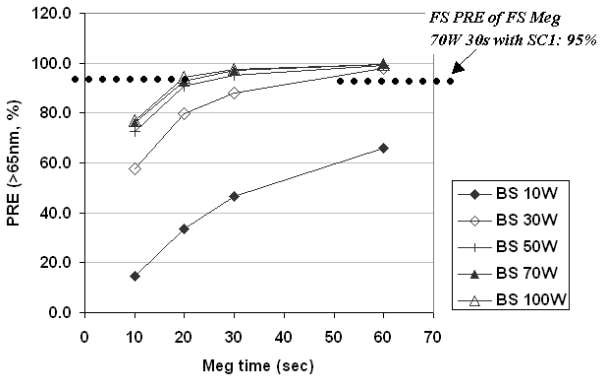


Fig. 7 Front side (FS) PRE in SC1 as functions of BS Meg power and time

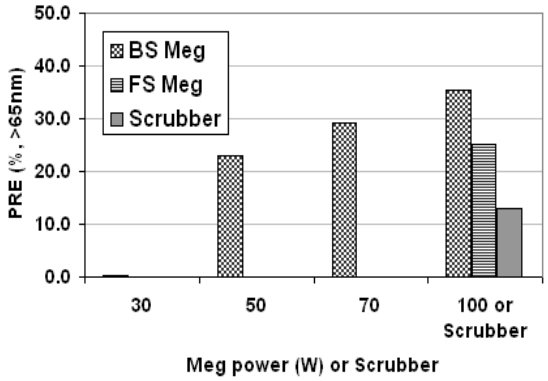
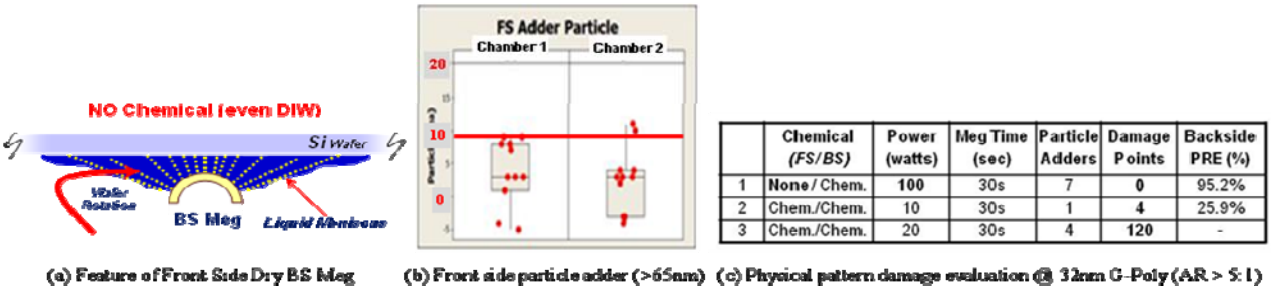


Fig. 8 Backside PRE comparisons on ESC marks when BS and FS Meg and a scrubber were employed

Marks. Testing was done to compare performance of the BS Meg to the FS Meg and a typical back side scrubber. Contaminated wafers were cleaned with SC1 for 30 seconds. BS megasonic power ranged from 30 to 100 Watts and FS megasonic power was directly applied to the front side of the wafer. The BS megasonic performed best with a PRE of ~ 35%. The FS meg PRE was ~ 25%, while the scrubber produced ~15% PRE. It is interesting to note that the BS megasonic outperformed the scrubber even at low power settings.

Advanced Applications

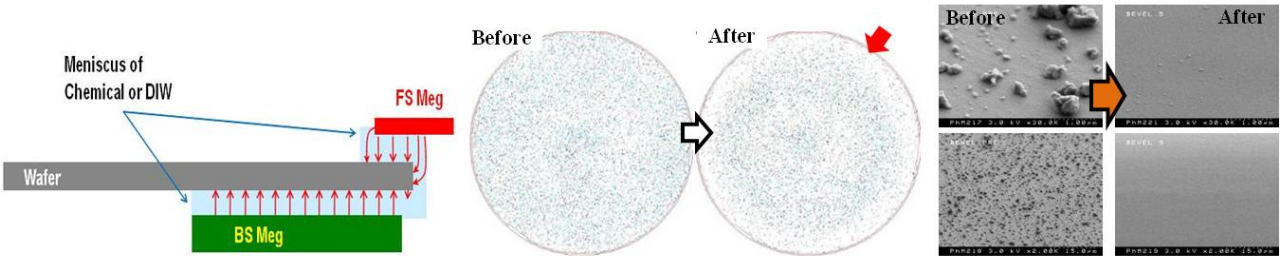
The system can be set up to clean without damage in applications where the front side has damage sensitive critical structures such as for 32nm gate-poly (AR>5:1) patterned wafers. This is accomplished by modifying the back side chemical nozzles and recipe configuration, and leaving the front side dry as shown in Fig. 9. While bubble explosions enhanced by only 10 Watts of megasonic energy could cause physical damage if the front side is wet, this does not happen even with 100 Watts of megasonic energy transferred through silicon wafer and air. Chemical/DIW supplied to the back side does not flow over the wafer edge to the front side during the whole process. The result is that only about 10 particles (> 65 nm) per wafer were added after the SC1 BS Meg clean.



	Chemical (FS/BS)	Power (watts)	Meg Time (sec)	Particle Adders	Damage Points	Backside PRE (%)
1	None / Chem.	100	30s	7	0	95.2%
2	Chem./Chem.	10	30s	1	4	25.9%
3	Chem./Chem.	20	30s	4	120	-

Fig. 9 Feature and evaluation results of front side dry BS meg process

As Fig. 4 illustrates, wafer edge and bevel clean are serious issues in need of a solution, so Akrion Systems developed a process that couples the Goldfinger® front side megasonic system (FS Meg) to its BS Meg process. Fig. 10 shows how this merged process works. The Goldfinger Meg is pulled out to the edge area and applied simultaneously with the BS Meg to reinforce cleaning efficiency at the edge and bevel area. Particle maps and SEM inspection before and after the clean confirmed that PRE at the edge and bevel was much improved.



(a) Feature of Edge/Bevel Focused Clean (b) Particle maps (>65nm) before/after clean (c) SEM images of wafer bevel area

Fig. 10 Feature and evaluation results of Edge/Bevel-Focused Goldfinger® Megasonic Clean

Electrostatic chuck (ESC) mark is a common backside contamination and remains after a variety of micro-fabrication processes such as lithography, ion implantation, plasma etch, film deposition, and inspection. ESC grips a wafer so strongly with the attraction of opposite charges of insulating and conducting substrates that it is not easy to remove chuck marks. This is especially true in the case of CVD, because the process temperature is relatively high (~400°C). It is more difficult to detach the marks so firmly adhered to the wafer. Hence, we pre-treated the wafer with dilute HF (DHF) just prior to BS Meg process in order to lift off the carbon-based contamination and boost efficiency of the BS Meg.

Fig. 11 back side particle maps show that severe circular ESC marks (contaminated in a CVD chamber) were almost completely removed by the process of DHF-BS Meg clean.

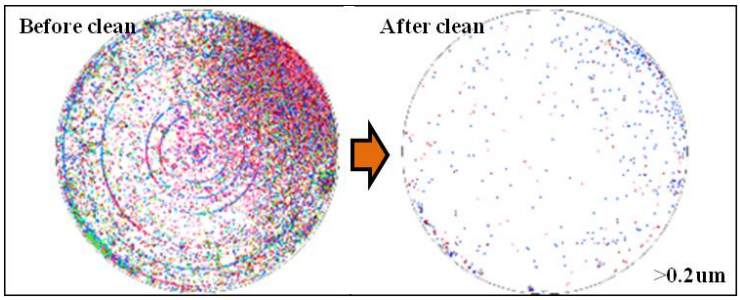


Fig. 11 Backside particle maps of the wafer contamintaed in CVD chamber before/after DHF-preteated BS Meg clean

Conclusions

In this study, an Akrion Systems' designed single wafer back side megasonic system was demonstrated to be capable of removing contaminants from both sides of a wafer concurrently. Depending on incoming wafer condition, the system is also able to clean the wafer back side only, thus protecting critical patterns from any physical/chemical damages. Furthermore, the system can be modified to reinforce cleaning efficiency at the wafer edge/bevel area. This was confirmed with PRE evaluation and SEM inspection. The experiment also revealed that DHF pre-treatment is helpful to remove strongly adhered ESC marks.

References

[1] HS Sohn, et al.: Removal of Backside Particles by a Single Wafer Megasonic System, 212th ECS Meeting, 2007.

[2] Motoya Okazaki, et al.: Wafer Edge Polishing Process for Defect Reduction during Immersion Lithography, Proc. SPIE, Vol. 6922 (2008)

[3] ITRS Roadmap 2008: Front End Surface Preparation Technology Requirements