EVALUATION OF ADVANCED PRE-GATE CLEANINGS

C. Cowache, P. Boelen and I. Kashkoush
AKrion *6330 Hedgewood Dr. 150 - Allentown PA 18106, USA*
P. Besson
STMicroelectronics *850 Rue Jean Monnet - 38921 Crolles, France*
F. Tardif
CEA Leti*, 17 Rue des Martyrs - 38054 Grenoble Cedex 9, France.*

ABSTRACT

In order to meet stricter wafer cleanliness requirements, emerging environmental concerns and more stringent cost-effectiveness criteria, wafer cleaning technology is moving slowly away from the conventional RCA-based processes. In this paper, the cleaning efficiency of different advanced pre-gate cleaning processes, all carried out in the same Wet Bench is compared. Dilute RCA, Diluted Dynamic Clean (HF/ Ozone- based process) and AFEOL (combination of diluted SC1, HF and Ozone chemistry) are evaluated in terms of metal and particle removal performance and major surface characteristics (surface roughness and minority carrier lifetime). Silicon and oxide consumption were also studied. Electrical evaluation was made on patterned Gate Oxide structures and electrical results from split lots with the optimized recipes are compared with those obtained with the conventional RCA process. Robustness of these three advanced cleaning processes is clearly established and we demonstrate that they perform at least as well as the standard RCA.

INTRODUCTION

Pre-gate cleaning is unanimously considered as one of the key parameters governing thin gate oxide integrity and hence final device performance and yield. However, despite increasingly stringent process demands (cf. SIA road map), the basic cleaning recipe has remained almost unchanged since 1965. The RCA clean [1], in its multiple forms, is still the choice of preference for FEOL cleaning sequences in IC manufacturing around the world. The reason is simple: concentrated NH_4OH/ H_2O_2/ H_2O mixture (SC1) performs very well for particle removal, and so does the HCl/ H_2O_2/ H_2O mixture (SC2) for metallic contaminants.

Recently cost-effectiveness and environmental concerns pushed considerable research efforts to optimize the RCA sequence and to develop alternative cleaning techniques. The first approach consists of diluting the SC1 and SC2 solutions, thus enabling important chemical savings at the same overall performances of the process. But implementation of diluted chemistries is not straightforward and there are many pitfalls to be avoided. Even then, some of the intrinsic limitations of the conventional RCA still remain valid for dRCA: high process temperatures (which is responsible for the major part of chemical consumption by evaporation) and multiple process steps. The use of diluted chemicals at room temperature represents another approach. The main new technological concepts have been introduced by IMEC [2], LETI [3] and professor Ohmi [4]. They all rely on HF-Ozone chemistry and include several sequences of ozonated water rinse(s) and dilute HF treatment(s). Basically the first Ozone step removes organics, noble metals, and oxidizes the wafer surface. The subsequent HF step removes the oxide as well as any embedded particles and metals. An additional ozone step is usually implemented to convert the hydrophobic surface to a more stable hydrophilic one. The reluctance of IC industry to adopt these relatively new cleaning strategies (even if very good performances have been extensively reported) suggests that an alternative intermediate approach is needed.

In this paper, a dilute RCA is proposed and the implementation of it in the wet bench is discussed. We present the latest technical advances in DDC. We also introduce a new Advanced Front End of the Line Cleaning, AFEOL, which consists of a combination of an HF-Ozone and a dilute SC1 chemistry (one could call this an intermediate approach between the dRCA and the DDC process).

The exact process sequences are detailed in Table I. The cleaning robustness of these different advanced pre-gate cleanings is extensively analyzed and discussed.

EXPERIMENTAL

All processes were conducted in a fully automated GAMA-1™ wet station from AKrion on 200mm, CZ, p-type, 7-10 Ω.cm wafers from SEH. The chemical tanks are recirculated and filtered. The SC1 tank is equipped with a Phaser Water Coupled Megasonic (peak energy ~ 5W/cm2) and the HF-HCl rinse tank with a Direct Coupled Megasonic (peak energy ~ 10W/cm2).
Some wafers were intentionally contaminated with different types of particles (with various Zeta potentials) or metals (with different electrochemical properties) to compare the Particle Removal Efficiency, (*PRE)* and the Metal Removal Efficiency, (*MRE).*
The contamination procedure for SiO_2 and Al_2O_3 particles is a short dip in DI water in which commercially available particles had been dispersed. Si_3N_4 contaminated wafers were obtained by dipping clean wafers in a static contaminated H_3PO_4 etch bath. Note that *PRE* is strongly dependent on initial counts and on the initial conditioning of wafers (cleaning before contamination). Therefore all experiments on contaminated wafers were carried out on samples from the same batch. Particle measurements were carried out on a TENCOR Surfscan 6200 (particle size: 0,16µm and upwards).
The procedure for metal contamination consists of an immersion in a SC1 solution (0,25/1/5 @ 25°C) previously spiked with standard Fe, Zn, Al, Ca, … solutions. Metallic contamination levels were detected by means of Vapor-Phase Decomposition TXRF (RIGAKU) and/ or VPD ICP (VARIAN). The detection limit of these techniques is ~10^9 atoms/cm^2 for the investigated elements (see Table II).
Non-contact methods for characterizing silicon surface properties after the cleaning process were used: Microwave PhotoConductivity Decay (µPCD) on a WT-85 Lifetime scanner from SEMILAB, and Surface Charge Profiler (SCP) on a SCP Model 100 from QC SOLUTIONS.
Wafer surface roughness was analyzed by means of Atomic Force Microscopy (Nanoscope III from DIGITAL INSTRUMENTS), rms roughness and number of "high peaks" being estimated from several 1µm × 1µm scans recorded in tapping mode. Some wafers were intentionally "roughened" in a 1% HF solution to generate "high peaks" on the silicon surface. Afterwards the "high peak removal ability" of the different cleaning processes was measured.
Etch rates and global process consumption of silicon and equivalent thermal oxide were determined with a 1280 KLA-TENCOR spectroscopic ellipsometer.
Finally, 70Å gate oxide structures of various area were patterned on split lots. Dry oxidation processes were prefered (no HCl species in the furnace) and conventional electrical tests were carried out on wafers after PolySilicon deposition and etch (test for EBD, QBD, Breakdown voltage, defect density).

RCA	**Time (min)**	**Goal**
SC1 0.25/1/5 @ 65°C	**10**	**Particle removal**
Hot rinse	**10**	**rinse**
SC2 1/1/5 @ 50°C	**10**	**Metals removal**
Hot rinse	**10**	**rinse**
Final rinse	**10**	**rinse**
IPA DRY	**7**	**Dry**
	57	

d RCA	**Time (min)**	**Goal**
dSC1 0.25/1/20 @ 65°C	**10**	**Particle removal**
Hot rinse	**7,5**	**rinse**
dSC2 1/0/250 @ 65°C	**10**	**Metals removal**
Hot rinse	**5**	**rinse**
IPA DRY	**7**	**Dry**
	39,5	

DDC	**Time (min)**	**Goal**
O_3 10ppm	**5**	**CHx + noble metal**
HF-HCl 1/1/100 @ 23°C	**0,5**	**Chem. oxide + metals removal**
Rinse (0.01% HCl)	**3**	**rinse**
O_3 3ppm	**7**	**Particle removal**
HF-HCl 1/1/100 @ 23°C	**0,33**	
Rinse (0.01% HCl)	**3**	**rinse**
O_3 5ppm	**7**	**Final Passivation**
IPA DRY	**7**	**Dry**
	33	

AFEOL	**Time (min)**	**Goal**
O_3 10ppm	**5**	**CHx + noble metal**
dSC1 0.25/1/20 @ 65°C	**7,5**	**Particle removal**
Hot rinse	**7,5**	**rinse**
HF-HCl 1/1/100 @ 23°C	**0,5**	**Chem. Oxide + metal removal**
Rinse (0.01% HCl)	**3**	**rinse**
O_3 5ppm	**7**	**Final Passivation**
IPA DRY	**7**	**Dry**
	37,5	

Table 1: *Description of different cleaning recipes studied.*
(Shaded cells indicate megasonic activation during the sequence)

RESULTS AND DISCUSSION

Particle contamination removal

We investigated both the particle addition on clean bare silicon wafers (initial count < 10 Lpds @ 0,16µm) and the PRE of different particle types.

- In the SC1 chemistry, particles are removed by the continuous oxidizing and etching effect of the NH_4OH/ H_2O_2 mixture, the ratio of these chemicals being the critical parameter since it determines the chemical dissolution rate of the surface layer to which the particle is attached (under-etching mechanism). While optimizing the dilute SC1 solution, the NH_4OH/ H_2O_2 ratio was kept constant which has proven to result in a similar etch behaviour of Si and SiO2 up to 0,25/1/500 [5]. An optimal working point at 0,25/1/20 was clearly established for the removal of all particle types we investigated (confirmation of a previous result obtained on Al_2O_3 slurries [5]).

As can be observed from fig. 1B, this optimized dilute SC1 (used both in dRCA and AFEOL sequences) outperforms the conventional concentrated SC1 step. This, on first sight, strange behaviour is explained by the fact that the propagation of megasonic energy is enhanced at higher chemical dilution ratios due to lower gas bubble formation [6].

- Earlier, HF-based chemistries (DDC) didn't perform as well as expected [7]; this was mainly due to hardware limitations. As can be seen on Fig. 1A, the use of new carriers drastically reduces the particle adders and the Direct Coupled Megasonic energy used during the Ozone + HCl rinse cycles has a major impact on the overall PRE. Under these conditions, excellent particle removal results are obtained by combining the under-etching effect (Ozone/ HF sequence) and the Zeta potential control (HF-HCl mixture).

Note that these hardware improvements also affect the AFEOL cleaning since it prevents any particle (re)contamination of the wafers after the dilute SC1 step.

Finally, if we compare the four cleaning processes (Fig. 1B), the conventional RCA is obviously the lesser performer.

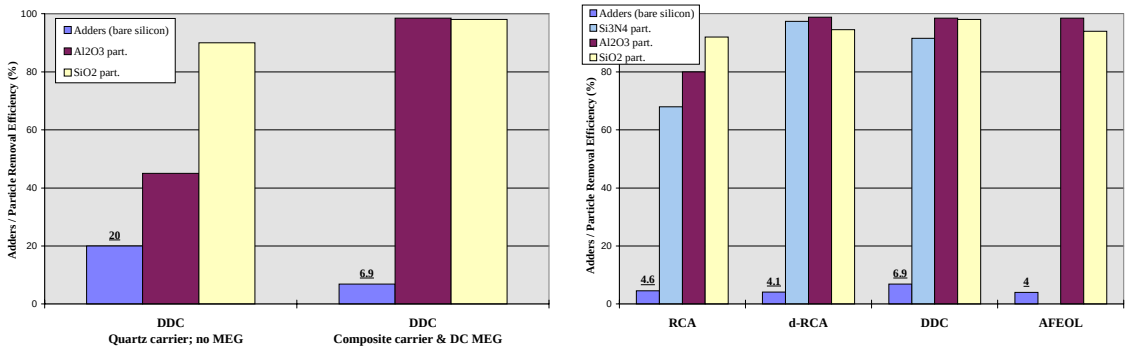

Fig. 1: *Particle performances measured @ 0.2µm (except adders @ 0.16µm).*
Left (1A): Improvement of HF-based chemistry. Right (1B): Comparison of different cleanings.

Recently, the understanding of the fundamental of particle// substrate interactions has progressed significantly (influence of ionic strength, Zeta potential, temperature, megasonic, dissolved gas, … [8]). Taking into account these parameters in the advanced cleanings cycles will be crucial for future developments. On the other hand, diluting the SC1 even more immediately raises some critical issues for chemical concentration control systems and megasonic technology (frequency, power) [6].

Metal contamination removal

Provided that high process temperature is maintained, strongly diluted HCl mixtures (up to 1/1000) are as effective in the removal of metals as the standard concentrated SC2 solution [9,10]. Optimizing the dilute SC2 solution, we fixed the HCl/ H_2O_2/ H_2O ratio at 1/0/250 (peroxide is completely left out) and increased the temperature to 65°C (pH ~1,4). This moderate dilution ratio enables us to keep the chemical

concentration in the bath under tight control by conductivity control (ICE™ regulation system) with a bath lifetime exceeding 2 days.

- Metallic contamination levels on cleaned "out of the box" wafers (VPD-TXRF or VPD-ICP measurements) are below detection limits of these techniques for all four cleaning processes. Table II presents the residual contamination levels measured after cleaning wafers that were first contaminated in a "spiked" SC1 solution. As is shown, all processes indicate good and even excellent abilities to remove high initial contamination levels (up to 10^{13} at./cm^2). Unfortunately, since most of the residual levels are at or below the detection limits of the available analysis techniques, a relevant comparison between the MRE of the different cleaning sequences is impossible.

*1E9at/cm2	Ca	Fe	Cr	Ni	Zn
LLD	1.4	2.1	0.16	0.06	1.1
Init. cont. level	9300	2050	13	17	17500
Post RCA	6.8	< lld	na	0.64	< lld
Post d-RCA	< lld	< lld	0.25	0.28	< lld
Post DDC	1.5	2.6	0.48	0.18	< lld
Post AFEOL	5.3	2.5	0.53	0.18	< lld

Table II: *Residual metallic contamination levels (after cleaning intentionally contaminated wafers).*

- SCP and μ-PCD measurements were also carried out. Indeed these techniques are very sensitive to metallic contamination (especially to iron for μ-PCD) and can be used for controlling the cleaning robustness [11].

Surface lifetime data measured by SCP and μ-PCD are reported in table III (τ_{scp} correspond to surface recombination lifetime, $\tau_{\mu pcd}$ to minority carrier lifetime). A noticeable difference appears between the wafers which are treated with a RCA/ dRCA clean or a DDC/ AFEOL clean. The distinction is even more pronounced for initially contaminated wafers (initial contamination levels are the same as those given in Table II). This indicates that the residual metallic contamination for these two groups of processes is slightly different. However one should keep in mind that in a first order approximation, $\tau_{\mu pcd}$ is inversely proportional to iron concentration: $[Fe] = (\tau_{\mu pcd})^{-1} * 5.10^{11}$ [11]. Hence the difference of 50μs measured by μ-PCD only represents a variation from 2.5 to 3.3 $*10^9$ at./cm^2. As mentioned above, in this range, the variations are hardly detected by analytical techniques.

Life time (μs)	SCP "Out of the box" Wafers	μ-PCD "Out of the box" Wafers	μ-PCD Met. conta. Wafers
RCA	18	191	168
d-RCA	39	180	166
DDC	56	203	209
AFEOL	68	201	216

Table III: *SCP and μ-PCD Life-Time measurements.*
SCP characterization is performed just after cleaning. μ-PCD measurements are carried out after oxidation (a thermal process is required to drive the surface Fe into the bulk of silicon).

At this point we can conclude that there is no major metallic contamination (removal) concern for any of the cleaning processes: **Alternative cleanings perform as good as conventional RCA process**, at least to the $1*10^9$ at./cm^2 level.

In the case of DDC and AFEOL processes, the key feature is the presence of chlorides in both the HF step and the final passivation step. In the dilute RCA approach, the critical parameter is the temperature. However when diluting the SC2 even further, metallic (re)contamination during the final rinse can become an issue. Then the injection of trace amounts of HCl during the final rinse would be recommended.

Silicon Surface Roughness

To which extent Si surface roughness affects the gate-oxide integrity is still a controversial issue. Indeed when "unrealistic roughening" of the silicon surface is obtained (either by long treatment in BHF [12], or in hot DI water [13] or in alkali solution [14]), a yield loss is detected. On the other hand, the correlation between rms roughness and intrinsic oxide performances is not so clear when relatively smooth surfaces (low rms roughness) are involved [10]. This is actually the case since the rms roughness values we measured were between 0.9 to 1.3Å for RCA, dRCA or DDC clean and slightly higher for AFEOL ~2Å (HF RCA sequence also leads to ~2Å).
However what can drastically affect the intrinsic properties of gate oxide structures is the presence of high peaks on the silicon surface [15]. Therefore the ability of a cleaning process to smoothen an artificially roughened surface is very important. As is shown in Fig. 2, the DDC process is very effective from this point of view. The AFEOL cleaning is able to reduce the number of high peaks as well, but this is not the case for RCA nor dRCA process.

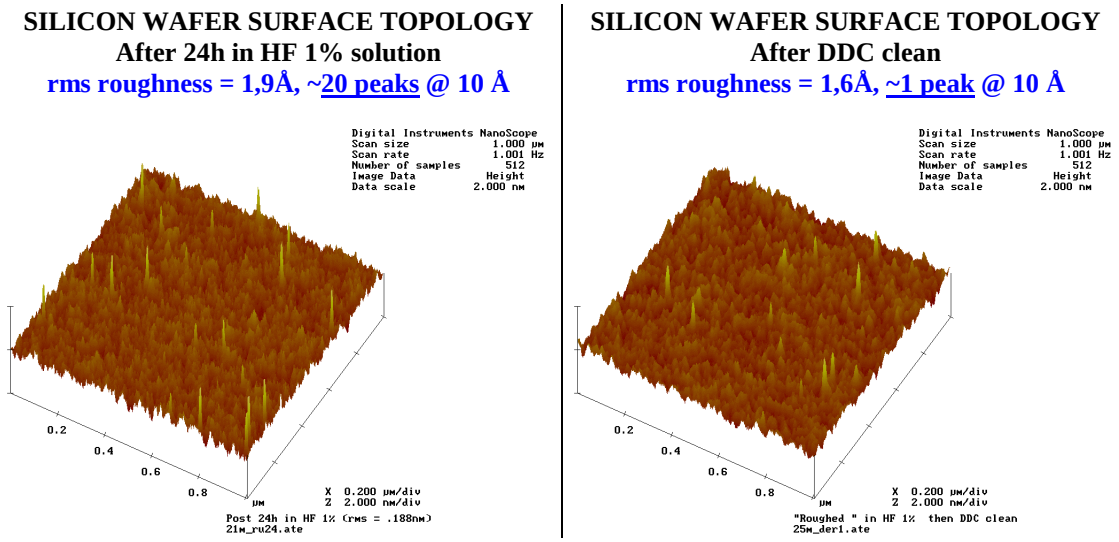

Fig. 2: *"High peak removal efficiency" of HF-Ozone based chemistry.*
Left side: artificially roughened sample with more than 20 peaks higher than 10Å on the silicon surface.
Right side: same sample after the DDC clean; just one peak higher than 10Å is remaining.

It was demonstrated earlier that strong oxidants such as Ozone or SPM drastically reduce the number of high peaks [15]. The occurrence of two active **Ozone steps** in DDC explains its ability **to smoothen the surface** and "cut" the high peaks.

Silicon and oxide consumption

For future generation devices and especially in the case of Silicon On Insulator technologies, tight control of oxide and silicon consumption (both in terms of global consumption and reproducibility) will become an important parameter.
From Table IV, there is only a slight difference between RCA and dRCA' etch rates: this is consistent with the fact that the NH_4OH/ H_2O_2 ratio is the same in the two SC1 solutions. Note that silicon consumption is ~20Å, a value which is commonly recognized as a "criteria" to obtain good particle removal efficiency [16]. During the DDC process, only ~10Å of silicon is consumed, during the two oxidation steps by ozone [15]. We demonstrated earlier that since the etching mechanism is intrinsically self-limited, the silicon consumption is practically insensitive to process parameter deviation (temperature, ozone and HF concentration, process time) and very reproducible. This is not the case in SC1 chemistry since silicon and oxide consumption are very sensitive to the NH_4OH/ H_2O_2 ratio. Therefore these cleanings are far more demanding as regards chemical concentration and temperature control systems.
Unfortunately, the two clear advantages of the DDC process mentioned above are somehow counterbalanced by a relatively high oxide consumption due to the two HF steps. Work is in progress to validate a DDC recipe using a more diluted HF-HCl solution.

Finally, the AFEOL process which includes dSC1 and HF-Ozone steps also cumulates the corresponding etch rates.

	RCA	d-RCA	DDC	AFEOL
Silicon (Å)	20	21	12	25
Silicon Oxide (Å)	11.5	7	74	51

Table IV: Silicon and oxide consumption of the global processes.

Electrical tests

At LETI site for more than 3 years, split lots are run in order to compare the final electrical performances of 70A gate oxide structures. The oxide is grown using dry or wet oxidation process on either DDC- cleaned or RCA- cleaned wafers. For this study, the AFEOL and d-RCA processes have been included into the loop.

- The cumulative results of Charge to Breakdown measurements are shown in Fig. 3.

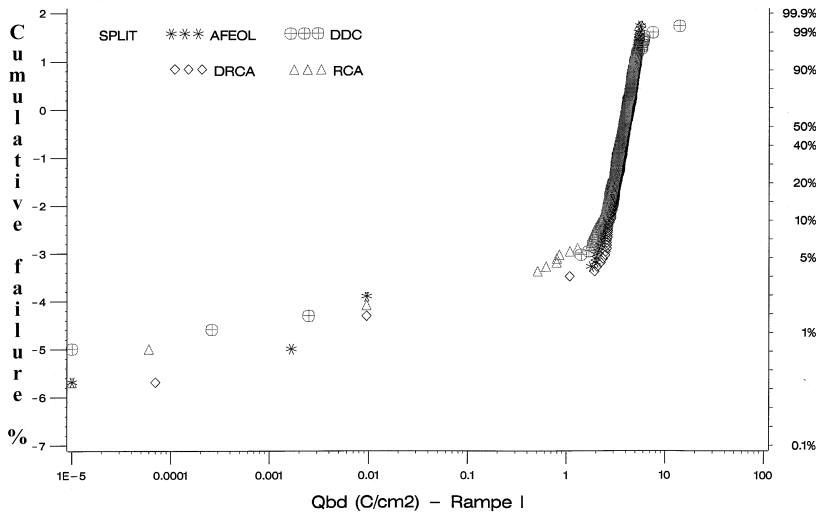

Fig. 3: *QBD distribution of 70Å gate oxide structures.*
(capacitor area = 0,07mm^2; 74 dies/ wafer; 4 wafers/ split lot).

The QBD distributions plots are very similar and there is no significant variation between the different splits (neither in the intrinsic breakdown part, nor in the extrinsic tail of the distribution). Note that electrical tests give sharp Weibull diagrams, indicating a very good uniformity of the gate fabrication process. Therefore, a direct comparison between the mean value of the distribution is meaningful.

- Mean QBD values are represented in Fig. 4, the left side of the graph corresponding to the Weibull distribution shown in Fig. 3.

From this graph, it seems that **Gate Oxide Integrity is slightly lower when the conventional RCA process is used**. This trend was confirmed on several batches, on capacitors of various sizes.

The good positioning of the DDC process was already demonstrated [15], and is due to the high quality of the chemical oxide layer grown in acidified ozonated DI water [17,18]. The AFEOL cleaning process ends with the same HF-Ozone sequence: the final chemical oxide being the same, the electrical performances are also very good. As regards the dilute RCA process, we have yet no clear understanding of why it performs better than the RCA clean.

On the right side of Fig. 4, we present mean QBD values measured on wafers which were first metal-contaminated, and then cleaned (with the four different sequences), oxidized and patterned.

As is shown, QBD are not much affected by the initial contamination, so the robustness of all four cleaning processes is clearly established. However, the relative positioning of the different recipes is rather "surprising". At this point, much more data are needed to statistically confirm the result. Work is in progress and new results will be presented during the conference.

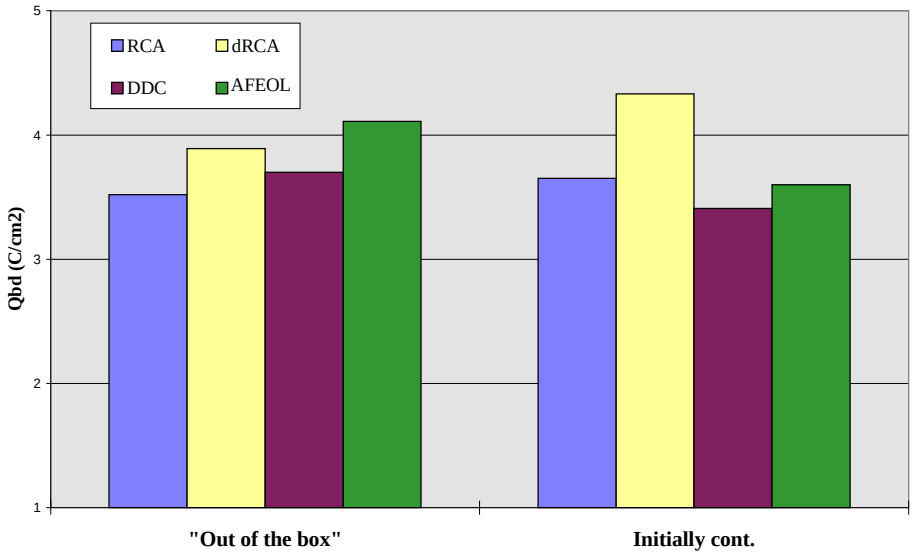

Fig. 4: *Comparison of Charge to Breakdown mean values on 70A gate oxide structures. (capacitor area = 0,07mm^2; 74 dies/ wafer)*
"Out of the box" stands for prime wafers which are cleaned and oxidize (4w/ split)
"Initially cont." concerns wafers which are first metal contaminated, then cleaned and oxidized (2w/ split).

CONCLUSION

Performances of the three alternative cleaning processes detailed in Table I have been measured and compared to the standard RCA clean.
On full sheet wafers, the Particle Removal Efficiency, the Metal Removal Efficiency and the "surface characteristics" we obtained with these advanced processes are at least as good as with the RCA process (more often better). Their robustness has been statistically demonstrated on patterned wafers by testing 70Å gate oxide structures from several batches. The electrical results confirm that the dRCA, the DDC or the AFEOL cleaning processes can be used as cost effective replacement for the conventional RCA clean, with the advantage of a much lower chemical consumption, lower footprint and higher throughput.
The new AFEOL sequence cumulates the reliability of the SC1 chemistry to remove the particles (actually an optimized dilute SC1) and the reliability of the ozone chemistry to insure a perfect passivation of the final silicon surface. Since the metallic contamination is also well-controlled, this process may represent a soft and reliable transition towards more advanced cleaning strategies (DDC process, IMEC-clean, ..).

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KEY WORDS

Page 1 - FEOL cleanings, dilute RCA, Diluted Dynamic Clean, HF-Ozone chemistries.
Page 2 - Particle removal, metal removal.
Page 3 - Megasonic.
Page 4 - Silicon Surface Properties, Surface Charge Profiler, μ-PCD.
Page 5 - Surface microroughness, Etch rates, Silicon consumption.
Page 6 - Gate oxide integrity, Surface Passivation.
Page 7 - Robustness, Cost of Ownership

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Dr. Christophe Cowache
***AKrion**, CEA LETI, 17 Rue des Martyrs - 38054 Grenoble Cedex 9, France.*
Tel. 33 (0)4 76 88 91 57
Fax 33 (0)4 76 88 50 03
e-mail: ccowache@compuserve.com