Effect of Pre-Cleaning on Texturization of c-Si Wafers in a KOH/IPA Mixture

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Experiments were performed to investigate the effect of pre-cleaning on surface texturization of mono-crystalline silicon in an KOH/IPA solution. Without appropriate pre-cleaning, surface contamination can cause the formation of pyramids with smaller sizes than those at the non-contaminated areas, leading to inhomogeneous texture features and reflectance non-uniformity on the wafer surface. Depending on the supplier, the surface quality and contamination level of wafers may vary and the pre-cleaning condition may need to be tailored to achieve consistent and desired texturization results.

Introduction

Texturization of crystalline silicon is one of the essential processes in solar cell manufacturing. A well-textured surface enhances the effectiveness of light absorption to a solar cell, which is deemed to be important for a cell's IQE (internal quantum efficiency) [1]. While a number of techniques have been developed for surface texturization, anisotropic etching with hot alkaline solutions is commonly used in the industrial production of c-Si (mono-crystalline silicon) solar cells [1,2]. With properly applied process parameters, wet chemical mixtures of KOH (or NaOH) and IPA (isopropyl alcohol) react with silicon, forming random pyramids on the surface of (100) oriented c-Si wafers and, accordingly, reducing the overall surface reflectance [3,4].

With the attempt to further optimize c-Si cell performance, the role of textured surface morphology (i.e. pyramid size, distribution, etc.) has been gaining increasing interest [5-7]. Depending on the cell structure, textured substrates featuring relatively large (or small) pyramid size are preferable for improved conversion efficiencies [5-7]. While most of the efforts are placed on tuning the texturing process parameters to control pyramid size, little attention has been paid to the variables of wafer surface qualities and the effects of pre-texture surface conditioning on the texturization results. In this article, by applying various cleaning conditions and using wafers from different suppliers, the effect of pre-cleaning on alkaline texturing of c-Si solar wafers is investigated and experimental results are discussed.

Experimental

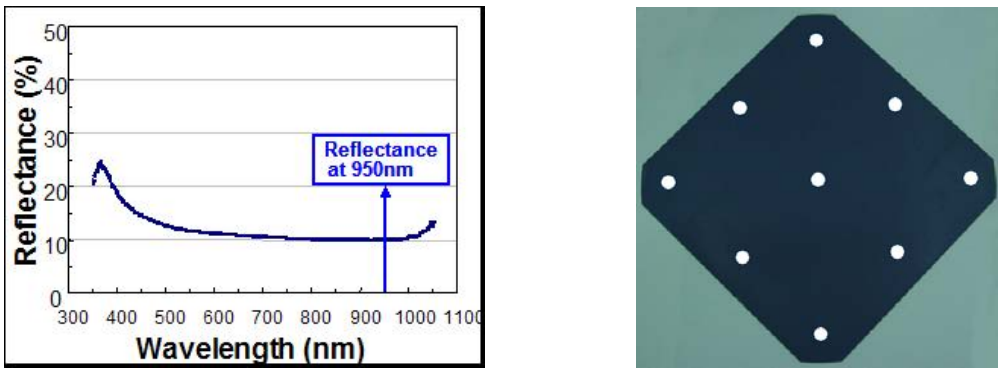
A number of c-Si solar wafers (Table I) manufactured by various suppliers were used in the experiments. The specific wafering process employed by each individual supplier is unknown, but the wafers are presumed to have gone through the typical process flow of wire-sawing, debonding, cleaning and packaging. The surface qualities and contamination levels are unclear but may vary with the supplier since sawing-marks and stains were visually observed on some of the wafers.

TABLE I. Information of the Solar Wafers Used in the Experiments.

Supplier	Wafer Size	Crystal Growth	Conductivity Type	Approx. Thickness
A	156 mm	Cz	P	210 μm
F	125 mm	Cz	P	180 μm
T	125 mm	Fz	N	240 μm
R	125 mm	Cz	N	200 μm
S	125 mm	Fz	N	220 μm

Wet chemical processes were conducted on a GAMA^{TM} wafer cleaning station in Akrion's Applications Laboratory. The typical sequence was pre-texture cleaning, texturization and post-texture cleaning. Split lots were run, prior to the texturization process, with various pre-clean conditions using alkaline, acidic or the combination. Texturization and post-clean was performed with a fixed condition of KOH/IPA and HF/HCl, respectively.

Silicon removal of the tested wafers was estimated by a weight loss measurement technique using a microbalance (with a 0.1 mg sensitivity) operated in a stagnant airflow chamber. Reflectance of wafer surfaces was measured using a spectrophotometer with an integrating sphere (probe size of 10mm). For convenience, the reading at 950nm wavelength was used to indicate the reflectance of a measured spot (Fig. 1a). To evaluate the reflectance uniformity, nine spots were measured across the surface of each individual wafer (Fig. 1b) and then an average value along with standard deviation (one sigma) was calculated. Surface morphology images were obtained using optical microscopy and SEM (scanning electron microscopy) techniques.



(a) (b)

Figure 1. (a) A typical reflectance spectrum and representative reading at 950nm for a spot measurement, and (b) nine-point measurements on a solar wafer with respect to the clock's hour-position.

Results

Effect of Pre-cleaning on Texturization Results

Using wafers from a supplier (supplier A), split lots with or without pre-clean and HF dip were run. The wafers were then processed together to receive the texturization and post-clean treatments. The test matrix and reflectance results are presented in Table II. It can be seen that, for each type of pre-cleans (including the no-clean), wafers with an HF-dip versus those without did not produce significant difference in terms of reflectance (average and standard deviation). HF-dip treatments prior to alkaline etching are

normally applied in semiconductor/MEMS device fabrication to remove the native and/or chemical oxide from silicon surfaces for etch-precision purpose. In the texturing of solar wafers, the etching depth requirement is not as stringent as in semiconductor processes. By counting when a huge amount of hydrogen bubbles started to emerge from wafer surfaces, the delay of silicon texturing due to the existence of a thin layer of native oxide was about 5 – 10 seconds in the present experiments, which is only a very small fraction of the entire texturization process time (i.e. 30 minutes). The HF-dip step, therefore, is apparently negligible in a solar wafer texturing process flow.

TABLE II. Test matrix of pre-cleans and corresponding reflectance results

Sample	Process			Rfl% (Avg) @ 950 nm	Rfl% (Stdev) @ 950 nm
	Pre-Clean	HF Dip	Texturization + post-clean		
A-21	SC1	Applied	BKM	9.22	0.10
A-22				9.47	0.11
A-23		Not Applied		9.41	0.07
A-24				9.50	0.21
A-27	Clean-1	Applied		9.42	0.15
A-28				9.18	0.10
A-29		Not Applied		9.18	0.14
A-30				9.31	0.13
A-33	Clean-2	Applied		9.34	0.10
A-34				9.46	0.09
A-35		Not Applied		9.39	0.13
A-36				9.36	0.12
A-39	Not Applied	Applied		9.05	0.10
A-40				9.05	0.29
A-41		Not Applied		9.07	0.32
A-42				9.10	0.13

Also, it was found that wafers without pre-cleaning showed a higher tendency of reflectance non-uniformity (i.e. standard deviation > absolute 0.2%), as indicated in Table II. To further demonstrate this, reflectance results in Table II along with the nine-point measurement data of each wafer are illustrated in Figure 2. Relatively dark spots (i.e. low reflectance areas) were commonly observed for those wafers textured without pre-cleaning, indicating noticeable texture non-uniformity.

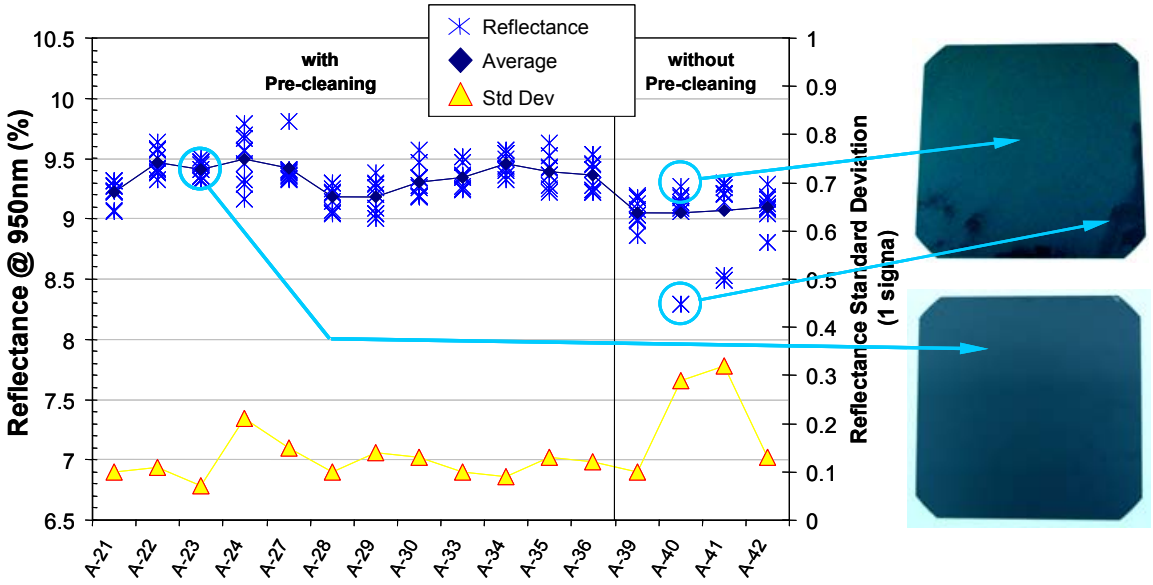
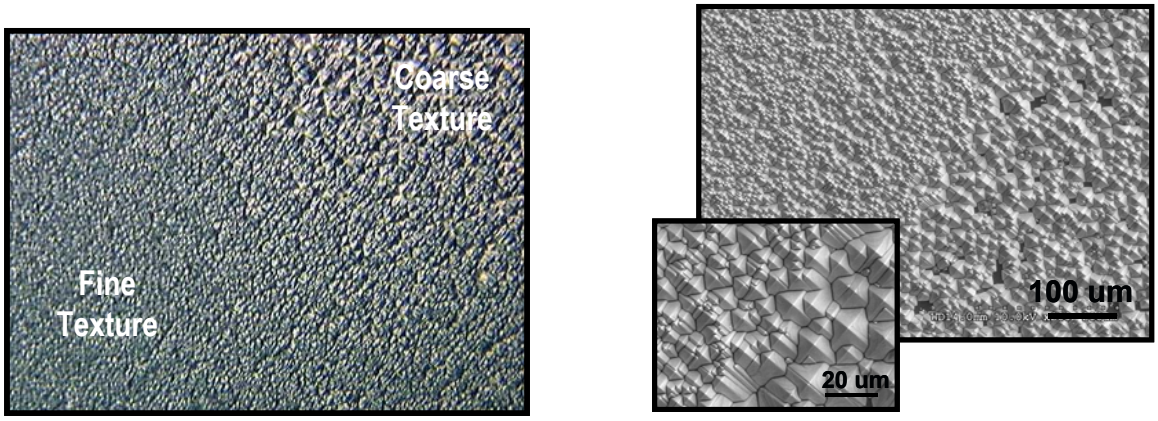


Figure 3. Nine-point measurement data showing the effects of pre-cleaning on the uniformity of reflectance across a wafer.

Examinations of surface morphology indicated that the reflectance variation is associated with the inhomogeneity of texture features, as shown in Fig. 4a. Further analysis with SEM showed that this resulted from an abrupt change of pyramid sizes from an area to another (Fig. 4b). The area of low reflectance was found to correspond with the area of small pyramids. The texturing inconsistency seemed to be due to the surface contamination of the solar wafers, since a pre-cleaned wafer surface intentionally touched with a cleanroom glove can show the dark patterns at the corresponding areas after texturization.



(a) (b)

Figure 4. Surface morphology of an inconsistently textured area; (a) optical microscopy image and (b) SEM image.

Effect of Silicon Etching on Pre-cleaning Efficiency

Additional experiments were performed on wafers from different suppliers. By skipping the HF dip, a number of test wafers from each group of F-, T-, R- and S-supplier were processed with pre-clean using the clean-1 recipe (versus a few wafers without the pre-clean) followed by the same texturization and post-clean. The wafers from different suppliers showed different texturing performance as follows (Table III).

TABLE III. Effect of Supplier wafers on Texturing Etch Rates and Reflectance Results

Sample	Pre-Clean Process	Texturing Etch Rate (normalized)	Average Etch Rate (normalized)	Avg Refl% @ 950nm	Refl% (Stdev)
F-13	Applied	1.00	0.99	9.23	0.07
F-15		0.98		9.48	0.10
T-11	Applied	1.07	1.04	9.38	0.08
T-18		1.06		9.41	0.08
T-21	Not Applied	0.99		9.65	0.25
R-13	Applied	0.76	0.76	9.83	0.43
R-14	Not Applied	0.75		9.57	0.29
S-10	Applied	0.81	0.82	10.06	0.21
S-11	Not Applied	0.83		10.10	0.16

- Wafers from group F and T exhibited consistent texturing etch rates and reflectance response with previous test results obtained from wafer group A. The texturing uniformity was fairly decent (reflectance deviation ≤ absolute 0.1%) except for the wafer that did not receive the pre-clean in advance (wafer #T-21, reflectance deviation = 0.25%).

- Wafers from group R and S showed significantly low texturing etch rates compared to the other groups (i.e. F and T). Also, regardless of the pre-clean, reflectance deviation of the R- and S-wafers was relatively high (mostly > 0.2%), indicating an inconsistent texturization across the wafer surface.

When examined with an optical microscope under the same magnification, the wafers from group R and S revealed noticeably finer texture features than the wafers from F- and T-group (Figure 5). The observations of low texturing etch rates and overall fine textures seemed to imply that bulk material issues could be a factor other than regional surface-contamination affecting the texturization results.

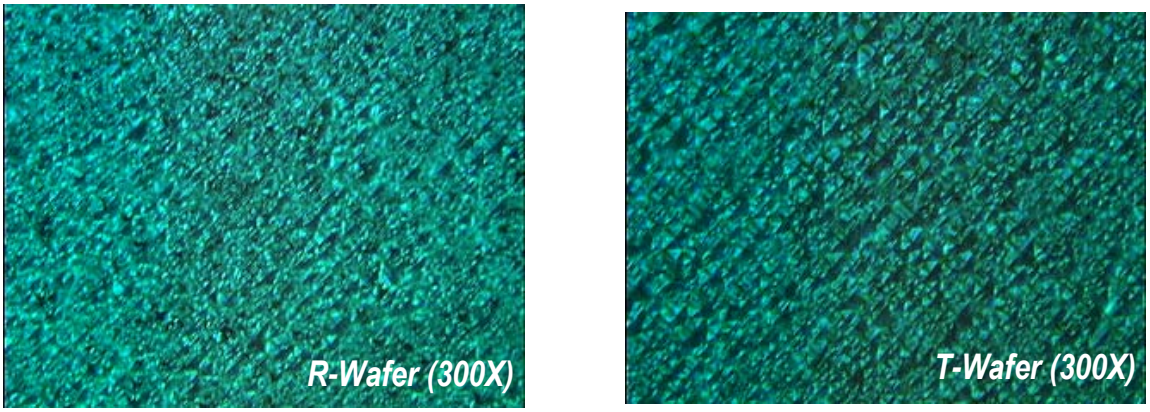


Figure 5. Wafers from R or S supplier (left) showing finer texturing features over the entire wafer surface than wafers from F and T supplier (right).

With cross-comparison of the information between Table I and Table III, no correlation can be found between the supplier-dependent texturing behaviors and the crystal growth method as well as conductivity type, suggesting that those observed are not primarily related with the bulk silicon material. Given that the SC1, Clean-1, and Clean-2 recipes mostly removed sub-micron level of Si from a wafer, it was postulated that a thicker layer of Si might need to be removed before a consistent texturing result can be obtained among the wafers from different suppliers. To verify the hypothesis, pre-texturing treatments with various etching conditions were applied to a set of test wafers from supplier F, S and R. The etching conditions were tailored to achieve different levels of Si removal prior to the application of the texturization process. The experimental results are presented in the following.

Figure 6 shows the texturing etch rate versus the total thickness of silicon removed from wafer surfaces by the pre-texture treatments. For better comparison, the texturing etch rate of all tested wafers are normalized against the one of an F-wafer without any pre-texture treatment (i.e. as-cut wafer). It can be seen that the texturing etch rate of F-wafers remained little change until greater than 10μm of superficial silicon had been removed by the pre-texture etching. This amount of superficial silicon is believed to be about the majority of the SDZ (saw damage zone) that has been induced by wafer wire-sawing processes. The high-energy state of the SDZ normally causes much more active etching reactions than the bulk material and thus increases the overall etch rate of texturization. Once the SDZ is etched away, the Si texturing etch rate slightly decreases.

In contrast to F-wafers, however, the R- and S-wafers showed relatively low etch rates at the as-cut state where most of the SDZ was in presence. The etch rates increased as more SDZ had been removed by pre-texture etching and eventually "converged" to the similar level of F-wafer texturing rates when approximate 3 – 4 μm of silicon had been pre-removed from the initial as-cut surface.

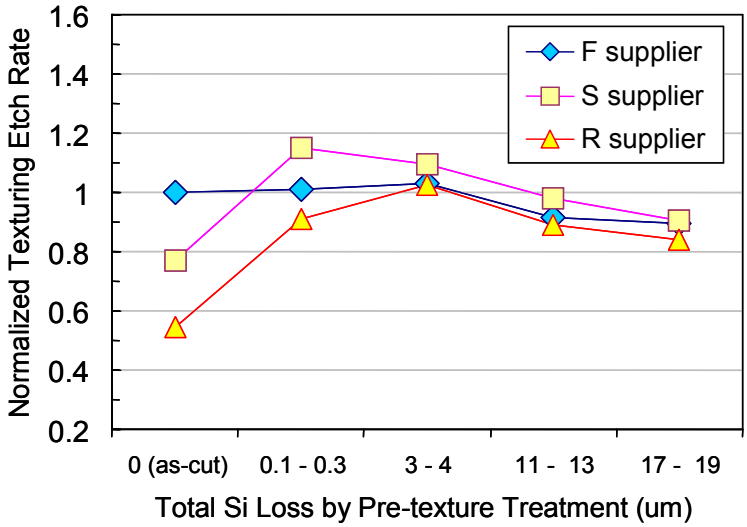


Figure 6. Effect of Si removal by pre-texture etching on the texturization etch rate

Texture features of the F-, R- and S-wafers versus the level of pre-texture etching are presented in Figure 7. For the as-cut surface, R- and S-wafers exhibited relatively fine features compared to the F-wafers, while all of the three groups showed similar surface textures after a sufficient pre-removal of silicon material.

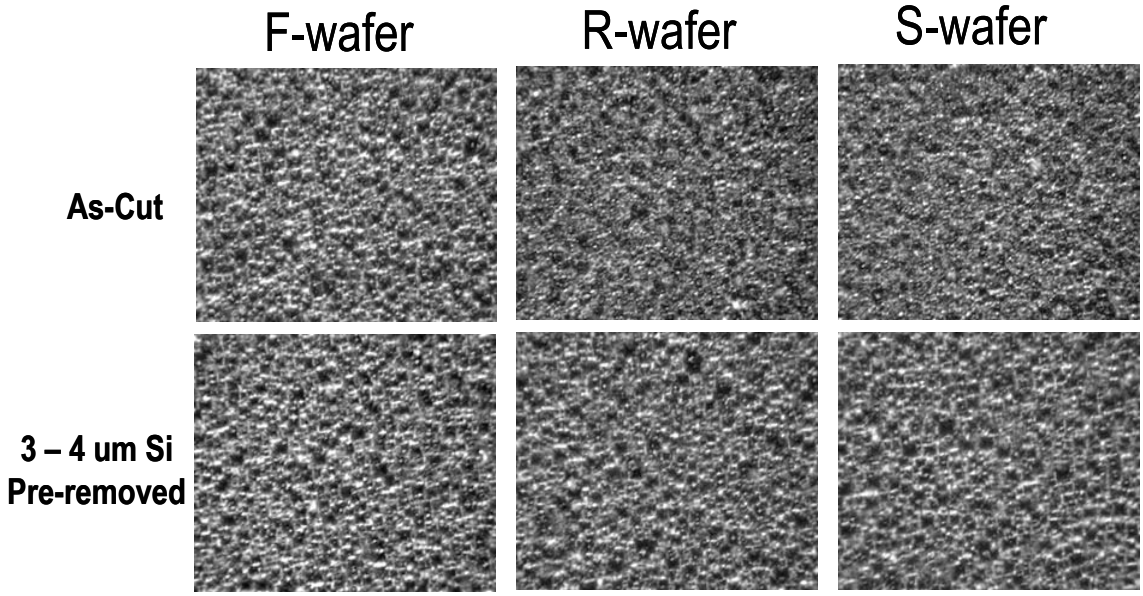


Figure 7. Texture features of three groups of wafers with different initial surface states; as-cut surface (upper row), and surface with 3 – 4 μm of silicon pre-removed (lower row).

Discussion

The experimental results have shown that the alkaline texturing of (100) c-Si wafers is strongly influenced by the initial surface state of the substrate. Gosálvez and Nieminen have developed a mechanistic model to delineate the nucleation and growth of pyramidal hillocks during anisotropic etching of c-Si, and used Monte Carlo simulation to predict the pyramidal texturing process with results consistent with published experimental observations [8]. They suggested in their model that impurities in the etching solution play a key role in the nucleation of the hillock by masking a superficial Si atom at the (100) plane to form the apex of a pyramid; once the apex atom is "stabilized" by the impurities, the (111) planes start to develop due to their relatively low etch rate to other major index planes such as (100) and (110), and a pyramidal hillock forms and grows. In the present work, micro-contaminants distributed on wafer surfaces seem to serve perfectly as the impurities for nucleation, enhancing intensive formation of pyramids on the contaminated areas. The inhomogeneous pyramid distribution, therefore, leads to reflectance non-uniformity across the wafer. As an effective chemistry to remove native oxide on Si surfaces, the HF-dip step, which barely etches Si, seems to be insufficient of removing the surface contamination and has little effect on reflectance uniformity. A pre-texturing treatment capable of producing both the cleaning and etching effects on silicon is therefore preferred. Since there are normally many micro-cracks appearing at an as-cut surface, the degree of surface contamination could be beyond the "surface level" and might vary largely with wafer suppliers depending on their wafering, cleaning and packaging processes. A pre-clean step may have to be adjusted against the surface qualities of incoming wafers to obtain consistent and desired texturization outcome. The pre-cleaning step, however, does not need to carry out a complete SDZ removal according to the experimental results.

Summary

By applying various cleaning conditions and using wafers from different suppliers, the effect of pre-cleaning on the texturization of mono-crystalline silicon solar wafers in a KOH/IPA solution was investigated. Experimental results indicated that with the lack of proper pre-cleaning, relatively small pyramids preferred to form at the contaminated areas and cause inhomogeneous texture distribution on wafer surfaces. The texture inhomogeneity can be revealed by noticeable variations of the reflectance across the wafer surface (e.g. one-sigma standard deviation > absolute 0.2% from a set of nine-point measurement data in this case). In addition, depending on the supplier, wafer surface qualities could vary so much that relatively aggressive cleaning/etching processes were required prior to the texturization to achieve consistent texturing performance.

References

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