CHARACTERIZATION OF C-SI TEXTURIZATION IN WET KOH/IPA AND ITS EFFECT ON CELL EFFICIENCY

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ABSTRACT: Wafer surface texturization has become a key process in solar cell manufacturing. This paper presents the experiments we conducted to study the effect of wet process in controlling the texturization parameters, e.g. dimensions and density. It is theorized that the pyramids' sizes, density and distribution correlate to the cell efficiency through maximizing the light absorbance. The data show that the higher the etch rate the higher the reflectance and the less distribution of the pyramids size. The efficiency was shown not to be strongly correlated to reflectance. However, the cell current Isc increases with smaller and uniformly-distributed pyramids. The results also confirm the dynamics of the process and the need for more in-depth study to fully understand the mechanism by which the texturization patterns and size could be better engineered.

KEYWORDS: Solar Cell Efficiencies, Texturization, Crystalline

1 INTRODUCTION

The development of highest efficiency lowest cost solar cells requires surface conditioning steps to maximize the light trapping properties and to reduce the recombination losses on structured interfaces [1-3]. The texturization of Si surfaces also leads to an increase in surface irregularities that result in an increase in recombination losses. It becomes critical that the damaged surface layers be removed to decrease the micro-roughness [1-5]. The photovoltaic process requires that the reflectance of light is minimized so that the generation of electrical energy is maximized. This requirement mandates that the silicon surface must be modified in a way that traps more light. Wet chemical processing is still the standard method used to texturize the wafer surface in solar manufacturing lines [6-8].

With increasing price pressure and COO concerns, tools can be specified to produce in excess of 3000 wafers per hour (wph). Tools are typically configured with multiple baths for the same chemistry and batch sizes of 200 wafers. Wafers are held in cassettes and moved automatically from bath to bath. Wafers are typically exposed to this harsh chemistry for 30 minutes to produce these random pyramids. In-line processing has met with limited interest due to the length of the equipment needed to support long process times.

Wet processes dominate the manufacturing base. There is extensive learning that has been applied to wet processing, allowing for high quality, reliable and productive tools. The materials themselves are readily available at high purity levels. While some might suggest this is a 'mature' process and thus has limited remaining upside, nothing could be further from the truth. In practice, it is this depth of understanding that allows for improvements to be made on a rapid basis. That's why immersion batch tools have incorporated features like advanced process control (APC), and micro-contamination avoidance and /or control.

Many papers have been published to explain the mechanism of silicon etching [5-8]. However, more work is still needed to fully characterize the texturization process so that optimum results are obtained. This paper outlines some insights into the mechanisms and parameters that control the texturization process and how to achieve the optimum results for a given cell line. The paper also includes discussion of pre-cleaning and final cleaning steps and their effect on the cell efficiency.

2 EXPERIMENTAL

p-type 156 x 156 mm^2 wafers were processed in Akrion Systems' R&D Laboratory. Wet chemical processes were conducted on a fully automated GAMA™ wafer etching and cleaning wet station. The typical sequence was pre-texture cleaning, texturization and post-texture cleaning. Split lots were run, prior to the texturization process, with various pre-clean conditions using alkaline chemistry, acidic chemistry or the combination of the two types. Texturization and post-cleaning was performed with a fixed condition of KOH/IPA and HF/HCl, respectively. Wafers were then sent to a solar fab to complete the cell manufacturing. The standard process flow is shown in figure 1.

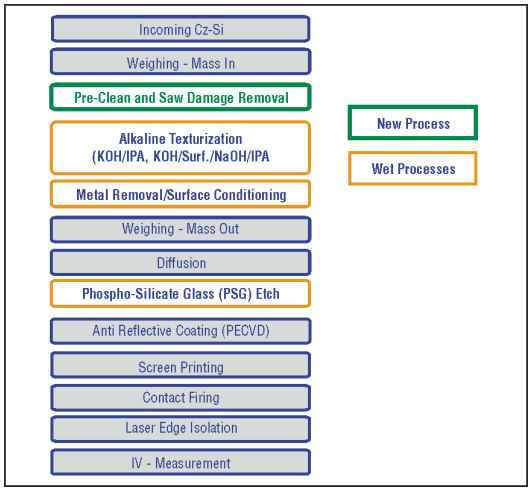

Figure 1: Standard screen print cell manufacturing process flow.

For the purpose of Design of Experiments (DOE), the following variables were investigated:

1. Amount of Si etched per side (5-20 µm)
2. Etch rate (as determined by concentration and temperature of KOH and IPA) (0.1-1 µm/minute)
3. Si-build up in the bath (5-500 mg/l)
4. Pyramid dimensions (1-20 µm)
5. Effect of final cleans (phobic/philic, HF/HCl

concentration and temperature)

Due to the dynamics of this process, each of these parameters was studied in a low (L), medium (M), high (H) level and the effect on the efficiency was recorded. The best-known method (BKM) for the final cleaning step was optimized and kept the same for all experiments for this part of the study.

3 CHARACTERIZATION

Surface characterization was done using different techniques including SEM, optical microscope, confocal micrscopy and spectrophotometery. Reflectance measurements were also made as shown below in the wave length range from 300 to 1100 nm. Some sample results are shown in Fig. 2. Cells were made and electrical parameters were recorded, e.g. efficiency, FF, Isc, Voc, Rs, Rsh.

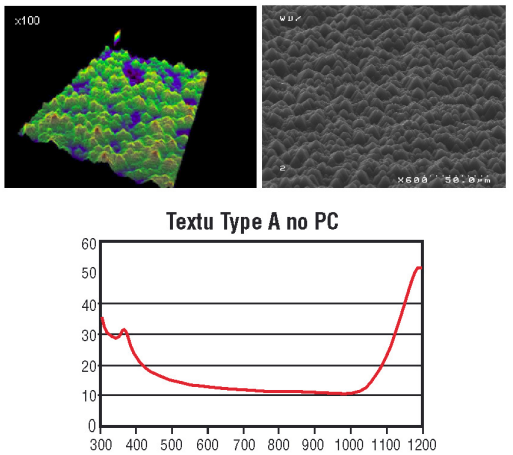

Figure 2: Texturization characterization using confocal microscopy (data courtesy of INES).

4 RESULTS AND DISCUSSION

Light management in the solar cell is critical. Silicon, a material with an indirect band gap, has a relatively low absorption coefficient. Efficient surface texturization, coupled with an anti-reflectance coating (ARC) can reduce reflectance losses from 35% to below 10%. As shown earlier in Figure 2, a well texturized surface reflects only 9.5% at 950nm compared to greater than 20% reflectance for an as-cut (untreated) surface.

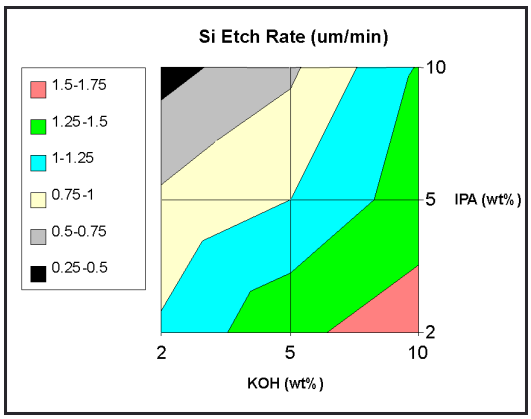

Figure 3: Si etch rates for various KOH and IPA concentrations.

Figure 3 shows the silicon etch rates in different KOH/IPA solutions at the same temperature. The etch rates increases as a function of KOH concentration while it decreases with increasing the IPA concentration. While IPA is used to facilitate the etching, it is also used to control the texturization process and creates the desired pyramids pattern. High KOH concentration reduces the pyramids size and densities i.e. higher reflectance as can be seen from figure 4.

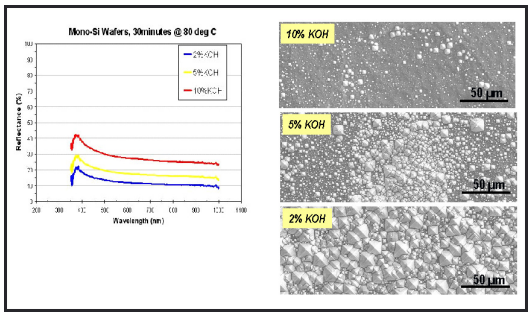

Figure 4: High KOH concentration reduces pyramids size and density.

The effect of pre-cleaning was also studied and a sample image is shown in figure 5. It can be easily seen that the contaminated areas have smaller pyramids dimension while uncontaminated areas have larger size pyramids. These contaminants work as a masking layer that suppresses KOH from reacting with silicon as readily.

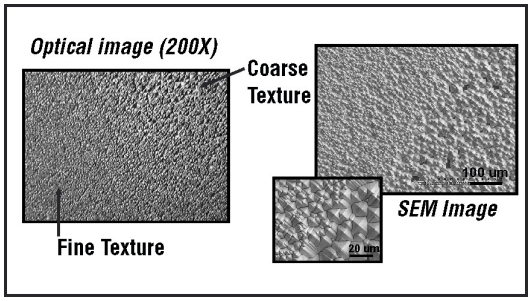

Figure 5: Contaminated wafers yield non-uniform texturization.

We present here a sample set of the results. The effect of the amount of silicon removed is shown in figure 6. As

can be seen from the data presented, cell efficiency increases to a maximum of 18.037% when removing about 9.0 µm of silicon. The efficiency then decreases as the amount of silicon etched increases to 12.57 µm.

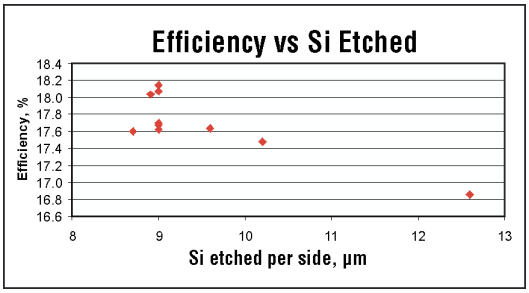

Figure 6: Correlation between solar cell efficiency and amount of silicon etched.

Increasing the silicon etched results in non-uniform and large size pyramid formation, i.e. higher reflectance or lower Isc. This is supported by the SEM images shown in figure 6a. The reflectance is also shown in figure 7 and plotted against the etch rate (ER).

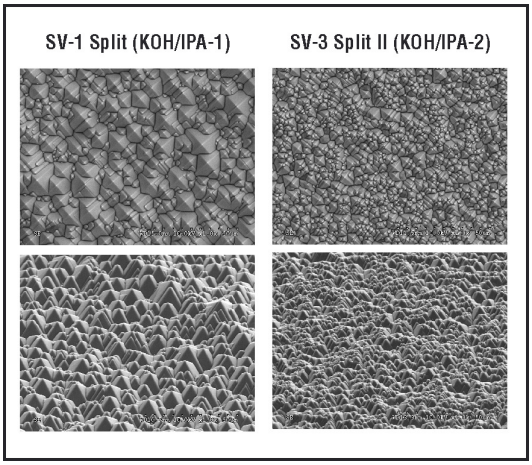

Figure 6a: Texturization pattern changes with the amount of Si etched.

The reflectance % is also shown in figure 7 at various Si etch rates. The higher the ER the lower the reflectance as can be easily seen from figure 7. Figure 7 also shows that the average pyramid height increases with etch rate. As a result, the pyramid's density is also lower with increasing etch rate as can be easily seen from figure 7. This is an important observation as cell different technologies may require different pyramid pattern and distribution as reported by EPFL in ref. [5]. The results are shown in figure 8.

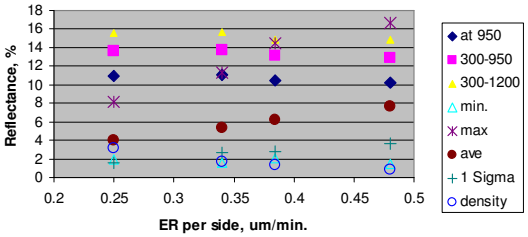

Figure 7: Correlation between etch rate and reflectance at various wavelengths (300-1100 nm).

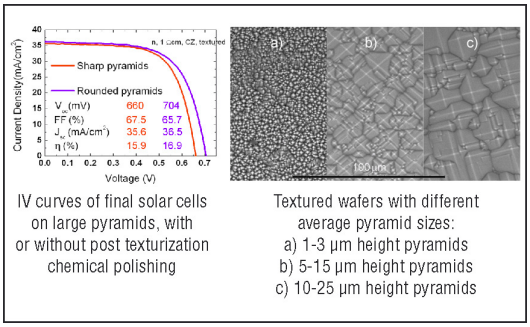

Figure 8: Different cell technologies require different texturization patterns [5].

More experiments were conducted to investigate the effect of these parameters and the data is summarized in Table 1. It would be ideal process engineering if we dial the parameters that give the maximum possible efficiency. Examining Table 1 closely, it appears that slowing the etch kinetics (lower etch rate), and producing uniformly and a small to medium-sized distribution of pyramids gives highest efficiency. In addition, the efficiency also increases with lower bath loading (Si content). High Si contents in the bath have a negative impact on wafer surface quality by introducing a source of contamination that will require aggressive subsequent cleaning steps to remove.

Parameter	Level	Test 1	Test 2	Test 3
Si Etched, µm/side	L	9	9	8
	M	11	12	11
	H	14	14	15
Etch Rate,µm /minute	L	0.2	0.25	0.15
	M	0.3	0.35	0.35
	H	0.45	0.45	0.50
Si Content, g/l	L	<1	<1	<1
	M	~2	4	1015
	H	30	30	50
Pyramid Dimensions, µm	L	3-6	3-7	3-6
	M	5-7	5-8	3-8
	H	7-11	7-11	7-11
Final Clean HF/HCL/O_3	L	Same POR	Same POR	Same POR
	M	Same POR	Same POR	Same POR
	H	Same POR	Same POR	Same POR
Efficiency, %	L	18.04	17.89	17.77
	M	17.34	17.11	17.01
	H	16.88	16.77	16.84

Table 1: Effect of wafer processing conditions on cell efficiencies, L (low), M (medium) and H (high).

After texturing, the wafers are rinsed with de-ionized water, cleaned in HF and/or HCl to remove metal impurities on the wafer surface, and then dried in hot air (heated clean dry air (CDA) or nitrogen). HCl removes surface impurities while HF removes the native oxide and any imbedded impurities in the oxide, leaving the wafer surface free of trace metals [8-10]. This results in an increased minority carrier life time. A metal signature of $< 5x10^{10}$ atoms/cm^2 could be obtained for Al, Cu, Fe, Mg, Mn, and Zn with this clean. This results in an increased minority carrier life time and improved sheet resistance. This HF-last process renders the surface H-terminated and is highly desirable prior to high temperature phosphorous diffusion.

	DL	A	B	C	D
Units: 1E10 atoms/cm²					
Aluminum (Al)	0.09	37	*	36	*
Calcium (Ca)	0.2	50	2.2	38	2.8
Chromium (Cr)	0.02	1.7	*	14	0.08
Copper (Cu)	0.02	63	*	2300	0.17
Iron (Fe)	0.09	10	0.22	35	0.25
Magnesium (Mg)	0.09	22	1.0	77	1.1
Nickel (Ni)	0.09	0.24	*	1.2	*
Potassium (K)	0.09	6.4	1.3	130	2.5
Sodium (Na)	0.09	17	0.65	8.8	0.74
Titanium (Ti)	0.09	0.84	0.19	3.0	0.24
Zinc (Zn)	0.09	1.5	0.12	3.4	0.53

* = Analysis revealed that the analyte was not found at or above the reporting limit. RL = Reporting Limit

Report Notes: Copper on surface of Wafer 1 is high relative to other three wafers.

Table 2: Typical metal signature after Akrion Solar's final cleaning step (A:Metals 1, B: Clean 1, C: Metals 2, D: Clean2, DL: Detection Limit).

As mentioned earlier, the final cleaning step was also optimized and kept unchanged during all experiments. Typical metal performance data is shown in Table 2.

5 CONCLUSIONS

Experiments were conducted to study the effect of wet process steps in controlling texturization parameters, e.g. dimensions and density. The data showed that reflectance decreases with decreasing pyramid height. Uniform distribution of the size of the pyramids is also advantageous in decreasing reflectance. The higher the etch rate the higher the reflectance and the less distribution of pyramid size. The efficiency is not strongly correlated to reflectance. However, current Isc increases with smaller and uniformly-distributed pyramids. Other down stream manufacturing steps can influence the results and vary significantly between solar lines and technologies. Based on the data, optimum conditions to boost efficiency appear to be the following:

a. Complete removal of saw damage (preferably done as a separate step)
b. Small and uniform pyramids size
c. Tight etch control (not affected by Si content in the bath or feed/bleed rates)

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